Compal Confidential

VSKTA Schematics Document

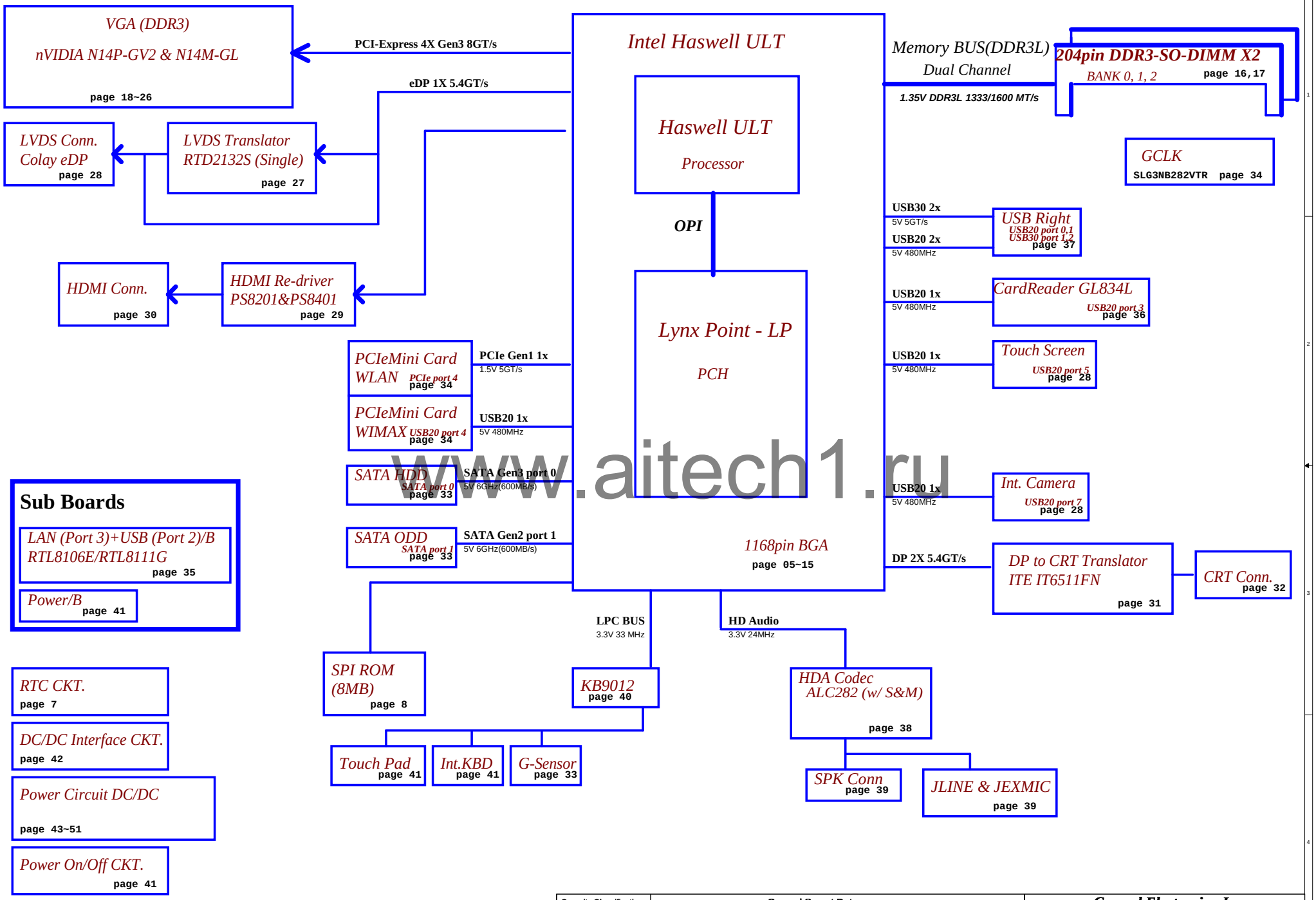
Haswell ULT with DDR3L

nVIDIA N14P-GV2 (Dual Rank)
nVIDIA N14M-GL

LA-9865P REV 1.0 Schematic

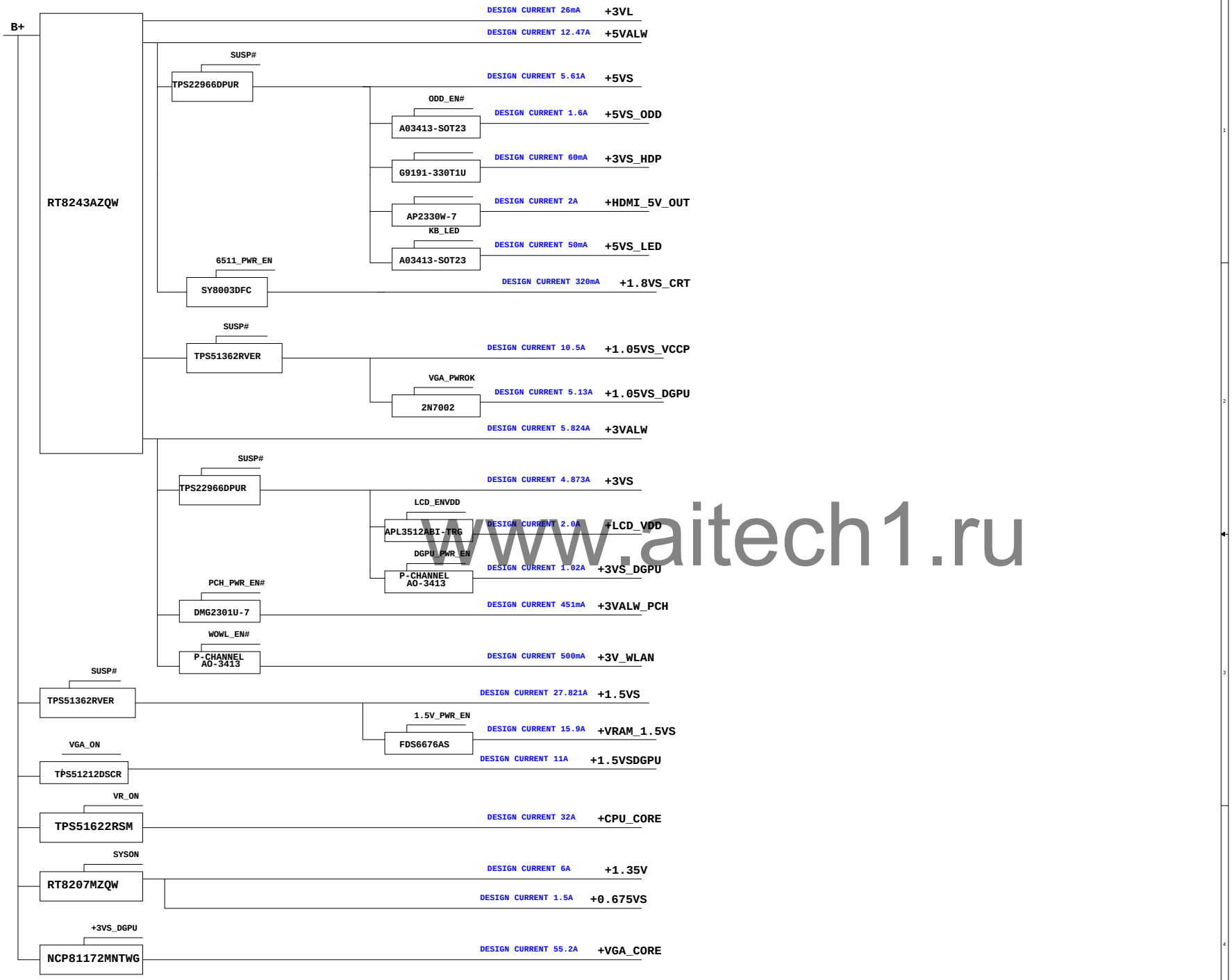
Intel Processor (Haswell)

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title: *Cover Page*	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size: Custom	Document Number: VSKTA	Rev: 1.0
				Date: Tuesday, March 19, 2013	Sheet 1 of 53



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: Block Diagram

File:	Document Number: VSKTA		Rev: 1.0
Date: Tuesday, March 19, 2013	Sheet 2 of 53		



Security Classification	Compal Secret Data		
Issued Date	2012/10/25	Deciphered Date	2013/10/05

Compal Electronics, Inc.

Title: **Power Map**

Size: Custom | Document Number: VSKTA LA-9865P MB | Rev: 1.0

Date: Tuesday, March 19, 2013 | Sheet 3 of 53

Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.5VALW +VSB	+1.35V	+5VS +3VS +1.8VS_CRT +1.5VS +CPU_CORE +VGA_CORE +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU +1.05VS_VTT
S0	0	0	0	0	0	0
S1	0	0	0	0	0	0
S3	0	0	0	0	0	X
S5 S4/AC	0	0	0	0	X	X
S5 S4/ Battery only	0	0	0	X	X	X
S5 S4/AC & Battery don't exist	0	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Smart Charger	12 H	0001 0010 b

Power	Device	HEX	Address

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9E H	1001 1010 b

Platform	SKU	CPU	PCH	VGA
				nVIDIA N13P-GL (N13PGL@)

BTO Option Table

Function	SKU	MIC	LAN				
description							
explain							
BTO							

Function							
description							
explain							
BTO							

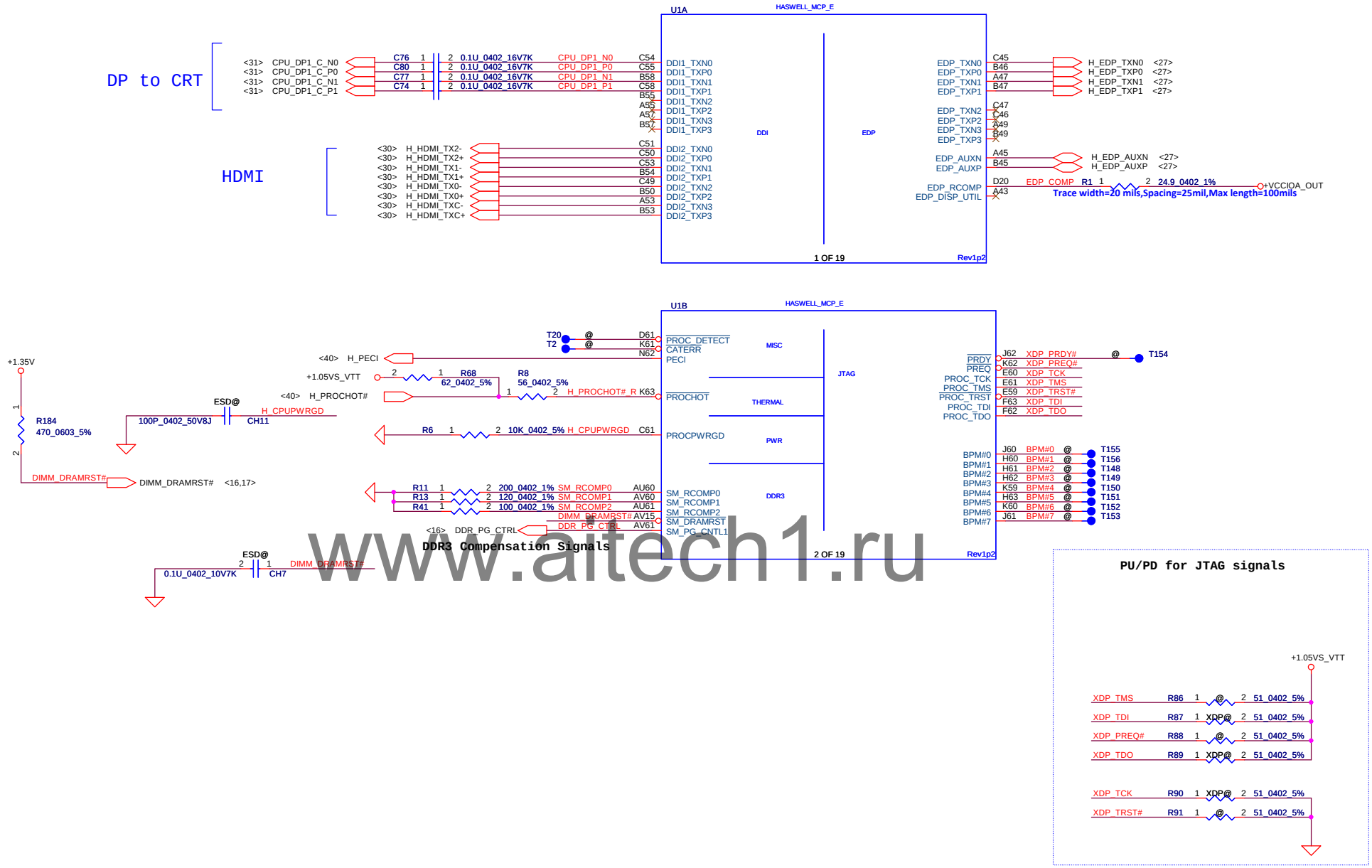
Function							
description							
explain							
BTO							

Function			
description			
explain			
BTO			

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

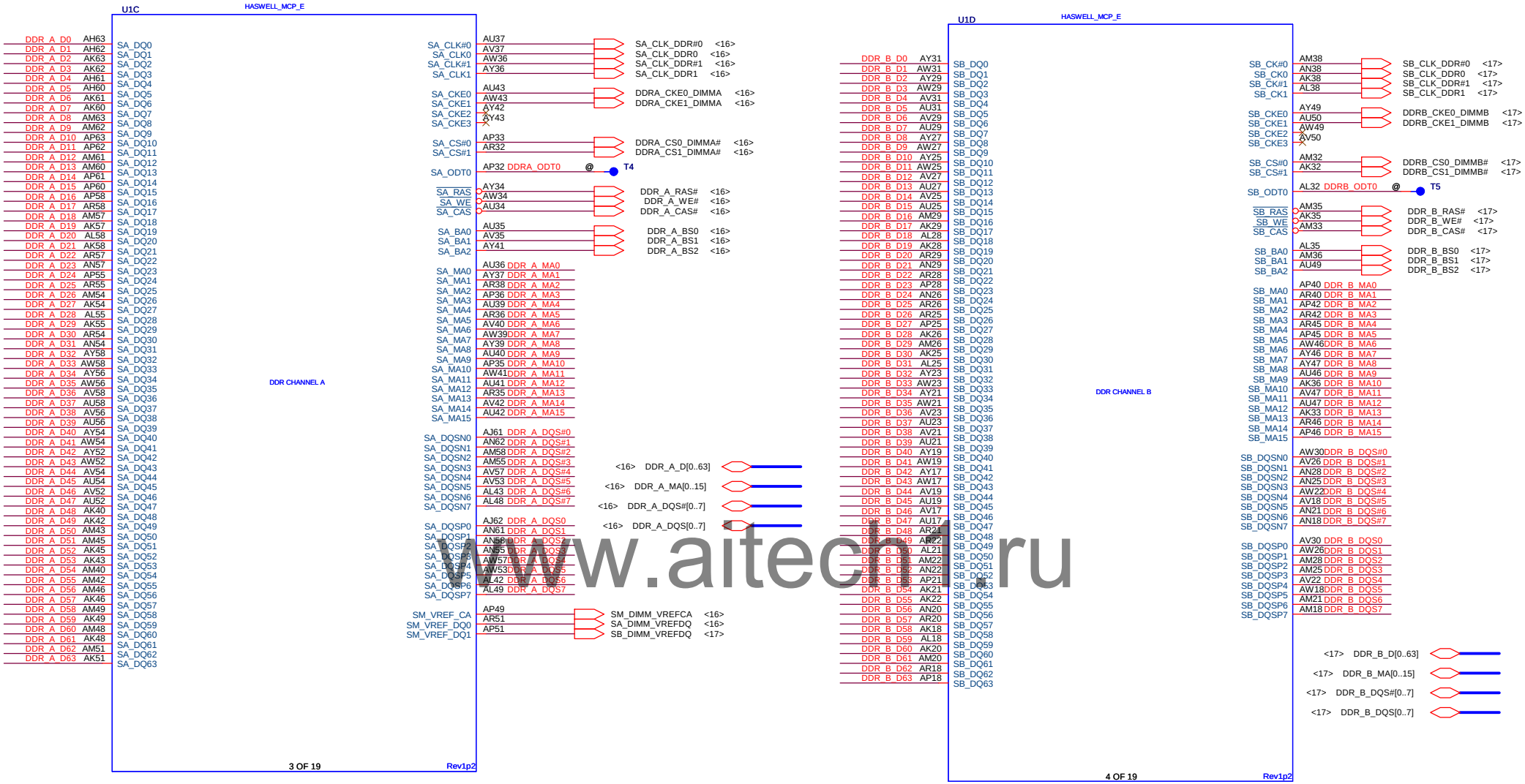
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/07/10	Deciphered Date 2013/07/10	Title: Notes List

Size: Custom	Document Number: VSKTA		Rev: 1.0
Date: Tuesday, March 19, 2013	Sheet 4 of 53		



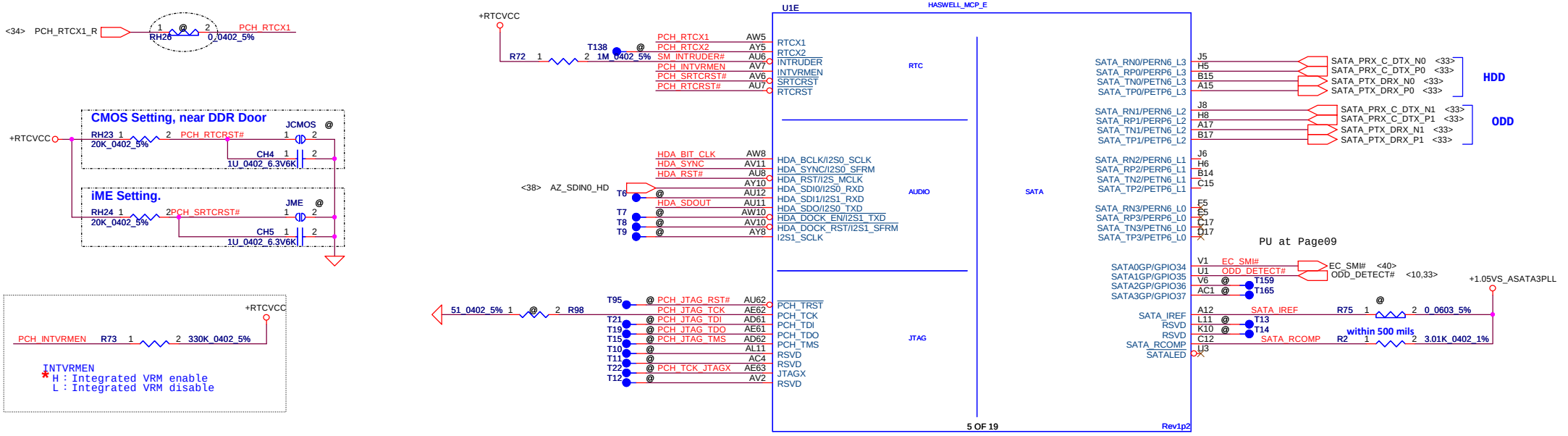
Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.			
Title	HSW MCP(1/11) DDI,MSIC,XDP		
Size: Custom	Document Number: VSKTA		Rev: 1.0
Date: Tuesday, March 19, 2013	Sheet 5 of 53		



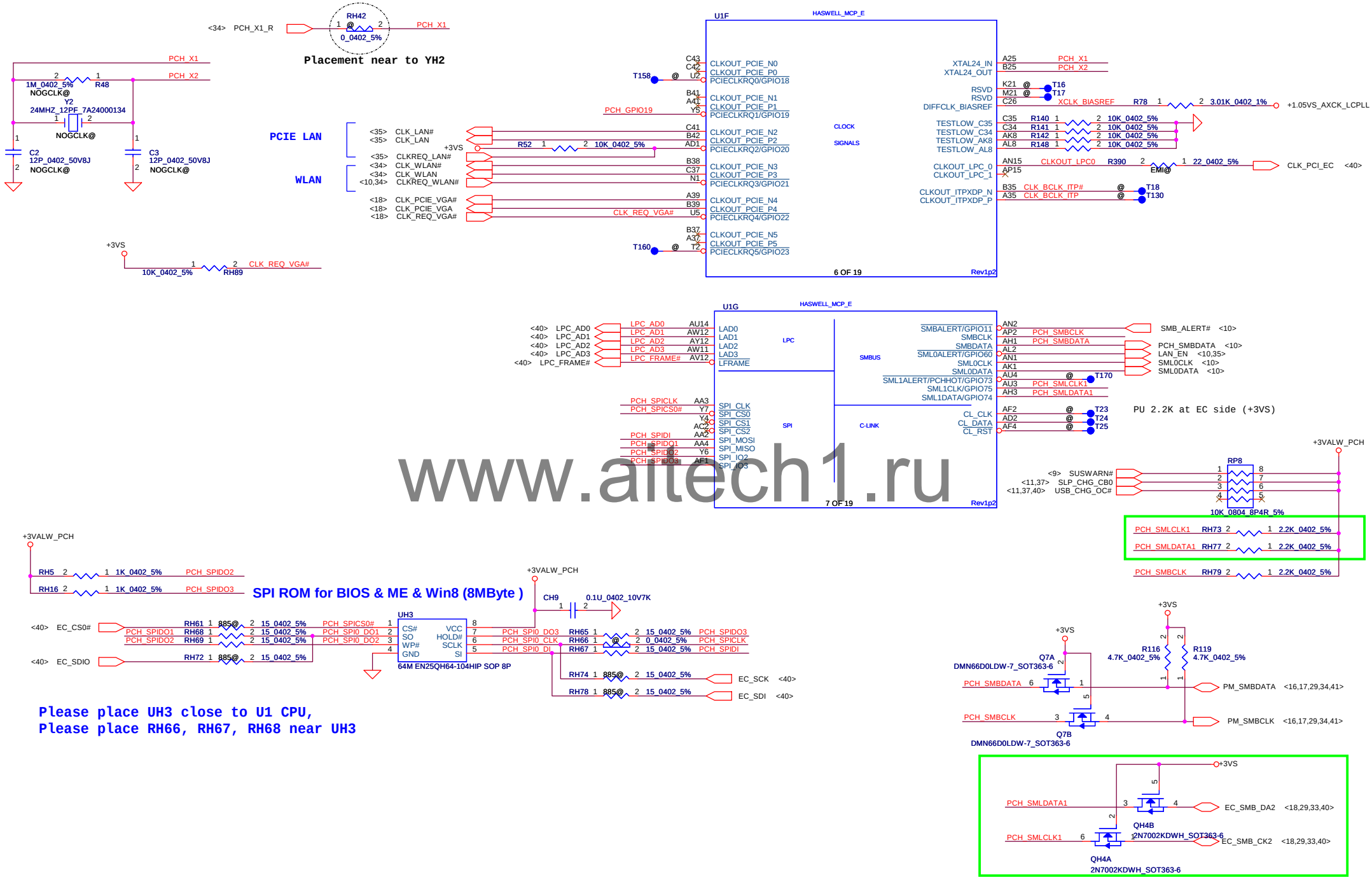
Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.		
Title: HSW MCP(2/11) DDRIII		
Size: Custom	Document Number: VSKTA	Rev: 1.0
Date: Tuesday, March 19, 2013	Sheet 6 of 53	



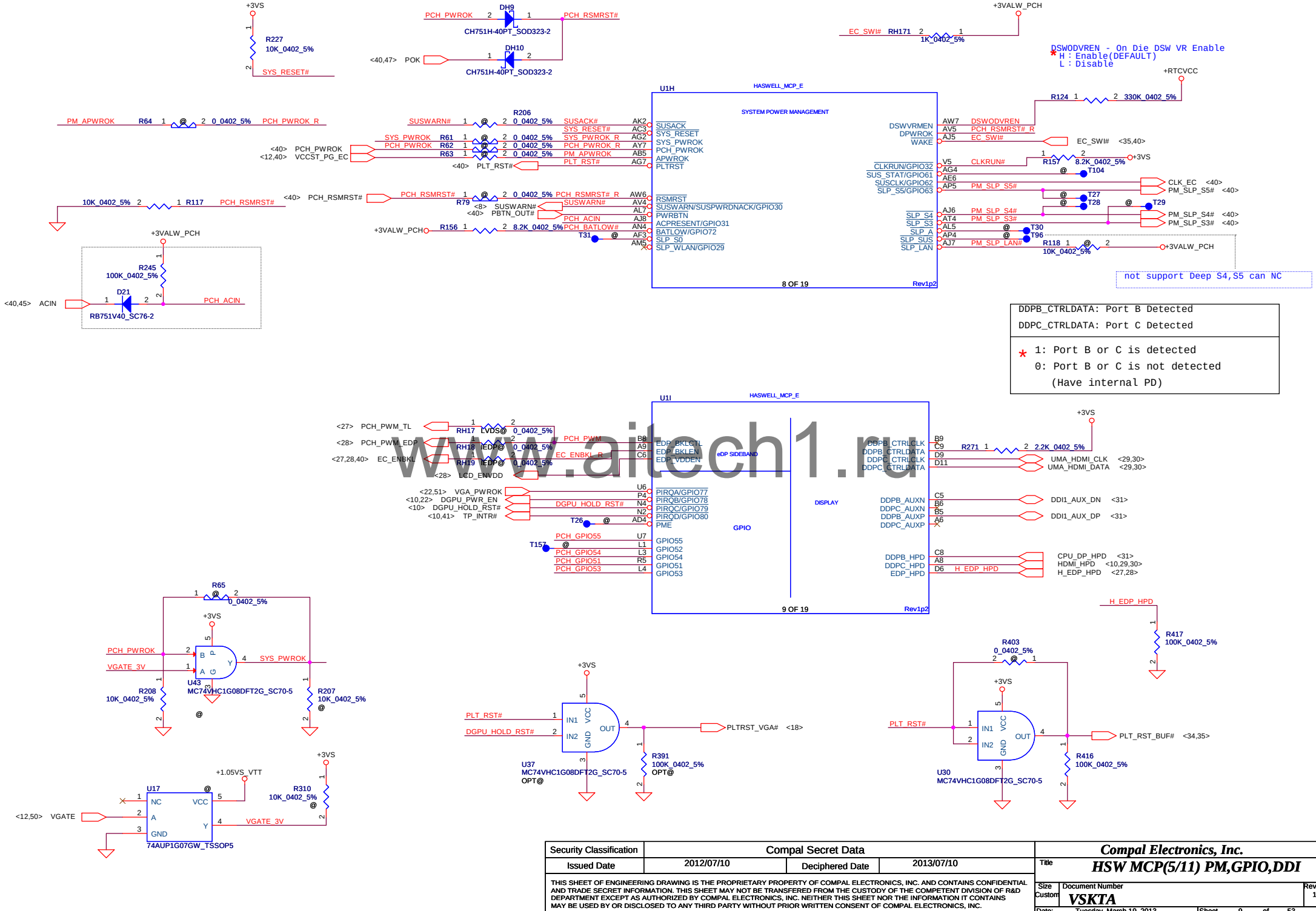
Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.			
Title	HSW MCP(3/11) RTC,SATA,XDP		
Size: Custom	Document Number: VSKTA		Rev: 1.0
Date: Tuesday, March 19, 2013	Sheet 7 of 53		



Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.			
Title	HSW MCP(4/11) CLK,SPI,SMBUS		
Size: Custom	Document Number: VSKTA		Rev: 1.0
Date: Tuesday, March 19, 2013	Sheet 8 of 53		



Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.			
Title	HSW MCP(5/11) PM,GPIO,DDI		
Size: Custom	Document Number: VSKTA		Rev: 1.0
Date: Tuesday, March 19, 2013	Sheet 9 of 53		

Note: need check all GPIO PU need or not after BIOS post

+3VS

RP23 10K_0804_8P4R_5%
- 7 DEVSLP0 — TP_INTR# <41,9>
- 6 SERIRQ
- 5 ODD_EN#

RP27 10K_0804_8P4R_5%
- 7 SPK_DET
- 7 ODD_DA#
- DGPU_HOLD_RST# <9>
- CLKREQ_WLAN# <34,8>

+3VALW_PCH

RP34 10K_0804_8P4R_5%
- LAN_EN <35,8>
- USB_OC#0 <11,37,40>
- SMB_ALERT# <8>
- SML0CLK <8>

RP9 2.2K_0804_8P4R_5%
- SLP_CHG_CB1 — SML0DATA <8>
- PCH_SMBDATA <8>
- USB_OC#2 <11,35,40>

+3VS

RP28 10K_0804_8P4R_5%
- PCH_GPIO27
- PASSWORD_CLEAR#
- ODD_DETECT# <33,7>
- DGPU_PWR_EN <22,9>

U1J HASWELL_MCP_E

T162 @	P1	BMBUSY/GPIO76	
T167 @	AU2	GPIO8	
	AM7	LAN_PHY_PWR_CTRL/GPIO12	
<40> EC_LID_OUT#	AD6	GPIO15	
<42> ODD_EN#	Y1	GPIO16	
<33> ODD_DA#	T3	GPIO17	
PCH_GPIO24	AD5	GPIO24	
PCH_GPIO27	AN5	GPIO27	
PCH_GPIO28	AD7	GPIO28	
PCH_GPIO26	AN3	GPIO26	
PASSWORD_CLEAR#	AG6	GPIO56	
T166 @	AP1	GPIO57	
PCH_GPIO58	AL4	GPIO58	
PCH_GPIO59	AT5	GPIO59	
<37> SLP_CHG_CB1	AK4	GPIO44	GPIO
PCH_GPIO47	AB6	GPIO47	
SM_DET	U4	GPIO48	
T163 @	Y3	GPIO49	
T139 @	P3	GPIO50	
PCH_GPIO71	Y2	HSIOPC/GPIO71	
T168 @	AT3	GPIO13	
PCH_GPIO14	AH4	GPIO14	
T169 @	AM4	GPIO25	
PCH_GPIO45	AG5	GPIO45	
PCH_GPIO46	AG3	GPIO46	
PCH_GPIO9	AM3	GPIO9	
<40> EC_SCI#	AM2	GPIO10	
<33> DEVSLP0	P2	DEVSLP0/GPIO33	
<39> SPK_DET	C4	SDIO_POWER_EN/GPIO70	
T136 @	L2	DEVSLP1/GPIO38	
PCH_GPIO39	N5	DEVSLP2/GPIO39	
<38> PCH_SPKR	V2	SPKR/GPIO81	

		THERMTRIP	D60 H_THERMTRIP#
		RCIN/GPIO82	V4 KB_RST# — KB_RST# <40>
		SERIRQ	T4 SERIRQ — SERIRQ <40>
CPU/MISC		PCH_OPI_RCOMP	AW15 PCH_OPIRCOMP — R145 49.9_0402_1%
		RSVD	AF20 @ T106
		RSVD	AB21 @ T32
		GSPI0_CS/GPIO83	R6 PCH_GPIO83
		GSPI0_CLK/GPIO84	L6 PCH_GPIO84
		GSPI0_MISO/GPIO85	N6 PCH_GPIO85
		GSPI0_MOSI/GPIO86	L8 PCH_GPIO86
		GSPI1_CS/GPIO87	R7 DGPU_PRSNT#
		GSPI1_CLK/GPIO88	L5 PCH_GPIO88
		GSPI1_MISO/GPIO89	N7 PCH_GPIO89
		GSPI_MOSI/GPIO90	K2 @ T135
		UART0_RXD/GPIO91	J1 @ T134
		UART0_TXD/GPIO92	K3 PCH_GPIO92
		UART0_RTS/GPIO93	J2 PCH_GPIO93
LPIO		UART0_CTS/GPIO94	G1 @ T114
		UART1_RXD/GPIO0	K4 — HDMI_HPD <29,30,9>
		UART1_TXD/GPIO1	G2 @ T111
		UART1_RST/GPIO2	J3 @ T133
		UART1_CTS/GPIO3	J4 PCH_GPIO3
		I2C0_SDA/GPIO4	F2 @ T132
		I2C0_SCL/GPIO5	F3 PCH_GPIO5
		I2C1_SDA/GPIO6	G4 PM_I2CSDA1 — PM_I2CSDA1 <41>
		I2C1_SCL/GPIO7	F1 PM_I2CSCL1 — PM_I2CSCL1 <41>
		SDIO_CLK/GPIO64	E3 PCH_GPIO64
		SDIO_CMD/GPIO65	F4 PCH_GPIO65
		SDIO_D0/GPIO66	D3 PCH_GPIO66
		SDIO_D1/GPIO67	E4 PCH_GPIO67
		SDIO_D2/GPIO68	C3 PCH_GPIO68
		SDIO_D3/GPIO69	E2 PROJECT_ID

10 OF 19 Rev1p2

JPW @

+1.05VS_VTT

R144 1K_0402_5%

H_THERMTRIP# — ESD@ CH12 0.1U_0402_10V7K

ESD@ ODD_DA# — CH6 180P_0402_50V8J

+3VS

PM_I2CSDA1 — R274 @ 1K_0402_5%

PM_I2CSCL1 — R272 @ 1K_0603_5%

+3VS

R306 10K_0402_5% UMA@

DGPU_PRSNT#

R219 10K_0402_5% OPT@

	GPIO87 DGPU_PRSNT#
DIS,Optimus	0
UMA	1

+3VS

R307 10K_0402_5% SM@

SM_DET

R220 10K_0402_5% NOSM@

Non-Harman detection

GPIO70 SPK_DET	0	ONKYO
	1	Non-Brand

GPIO48 SM_DET	BIOS setup	Speaker Type	BOM
1	S&M option	Harman/Kardon	SM@
0		Non Harman	NOSM@

PROJECT_ID

R215 0_0402_5% @

	GPIO69 PROJECT_ID
VSKTA	0
VSKAA	1

+3VS

R269 @ 1K_0402_1% — PCH_SPKR

SPKR / GPIO81 : NO REBOOT

1: ENABLED

* 0: DISABLED (Have internal PD)

+3VALW_PCH

R247 10K_0402_5% — EC_LID_OUT#

GPIO15 : TLS Confidentiality

1: Intel ME TLS with confidentiality

* 0: Intel ME TLS with no confidentiality (Have internal PD)

PCH_GPIO86 — R273 @ 1K_0402_5%

GSPI0_MOSI / GPIO86 : Boot BIOS Strap

1: ENABLED

* 0: SPI ROM (Have internal PD)

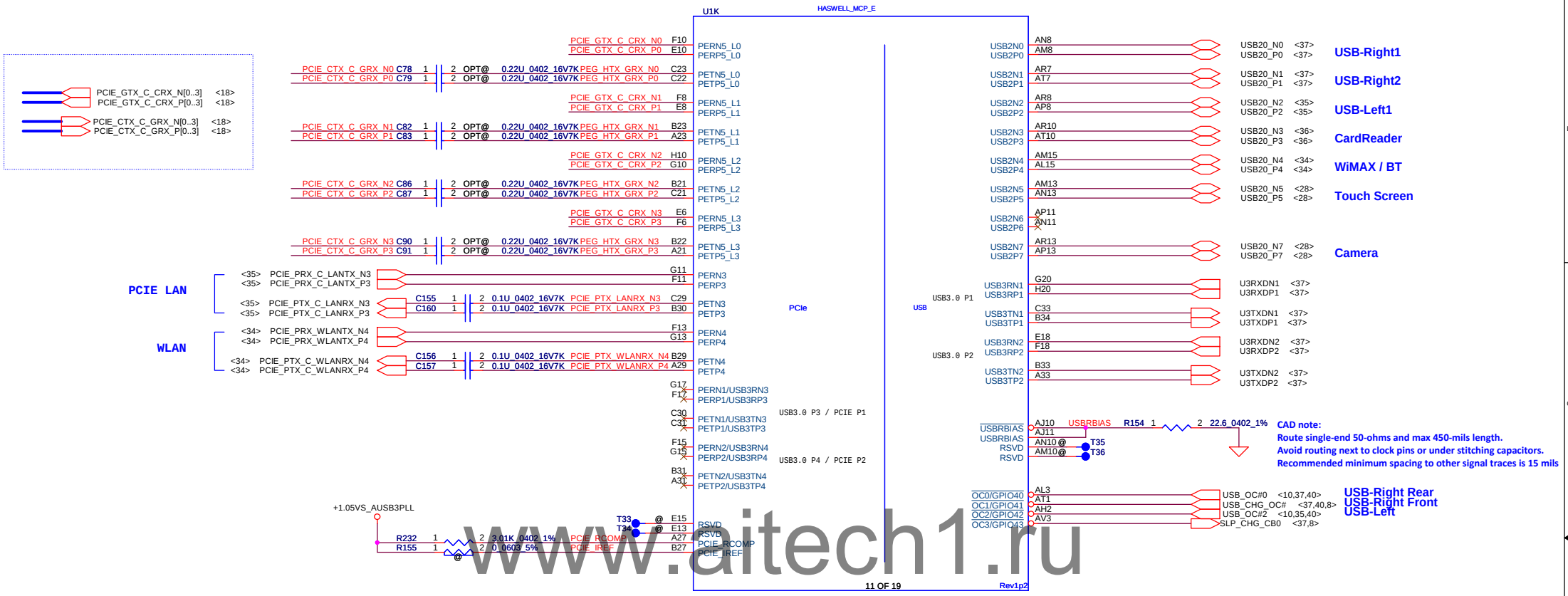
PCH_GPIO66 — R270 @ 1K_0402_1%

SDIO_D0 / GPIO66 : Top-Block Swap Override

* 1: ENABLED (Have internal PU)

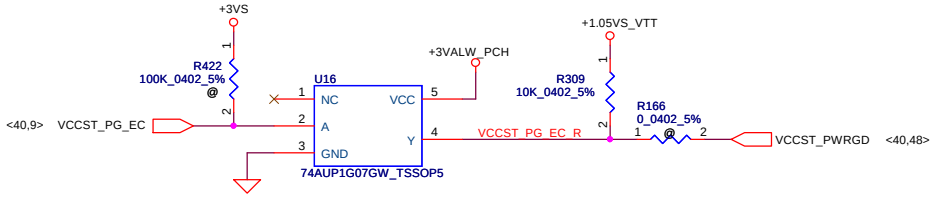
0: DISABLED

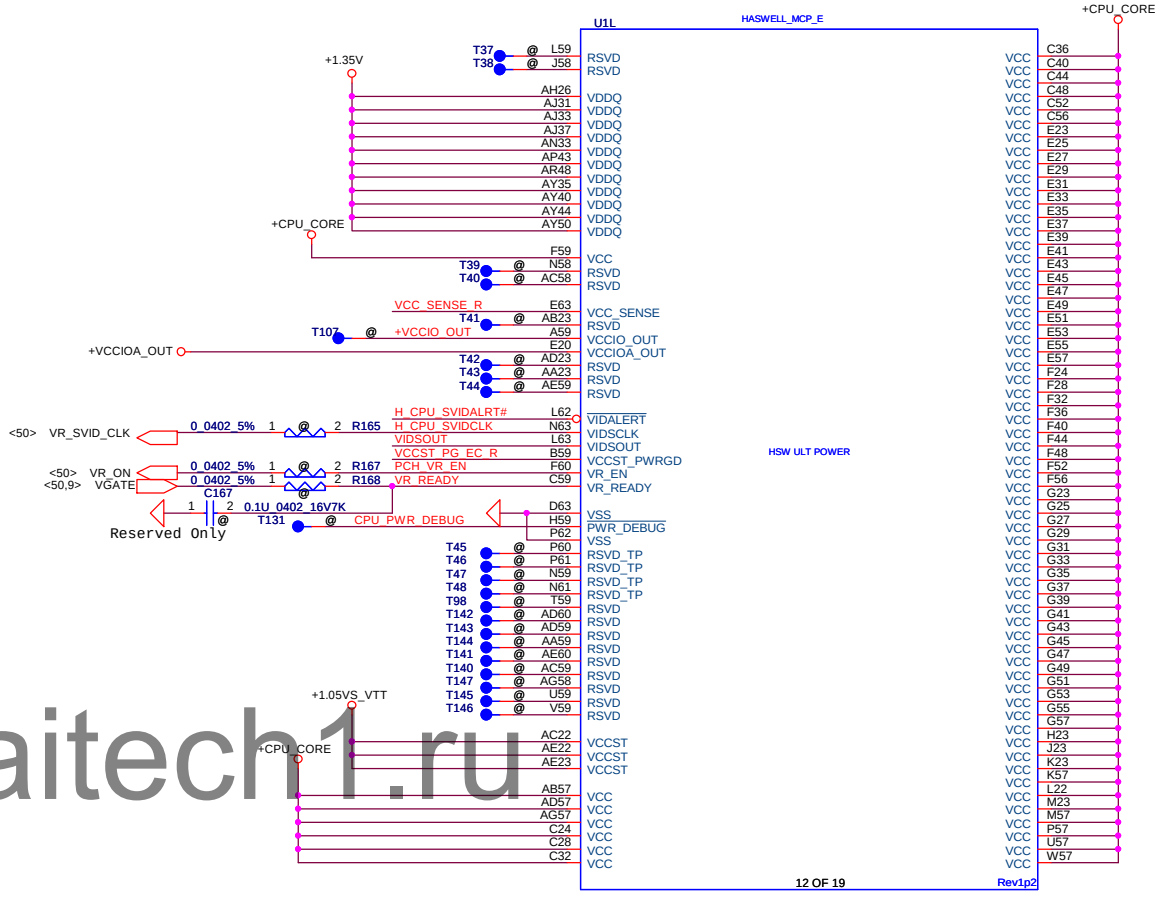
Compal Electronics, Inc.	
Title	HSW MCP(6/11) GPIO,LPIO
Size: Custom	Document Number: VSKTA
Rev	1.0
Date: Tuesday, March 19, 2013	Sheet 10 of 53



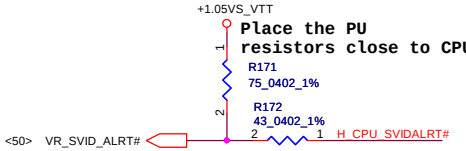
Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.	
Title	HSW MCP(7/11) PCIE,USB
Size: Custom	Document Number: VSKTA
Rev	1.0
Date: Tuesday, March 19, 2013	Sheet 11 of 53

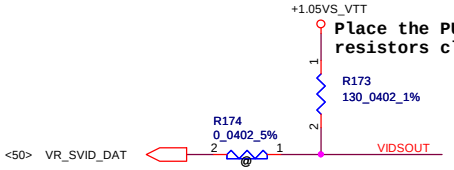


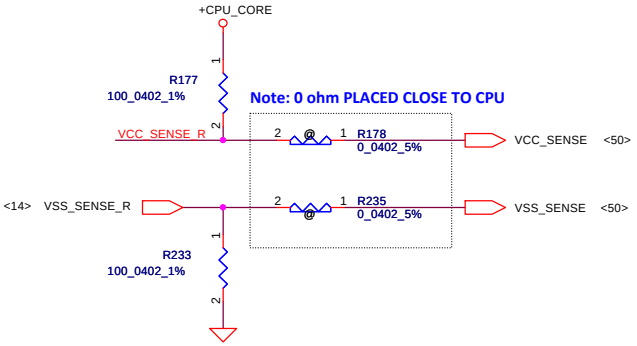


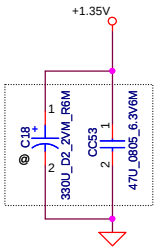
SVID ALERT



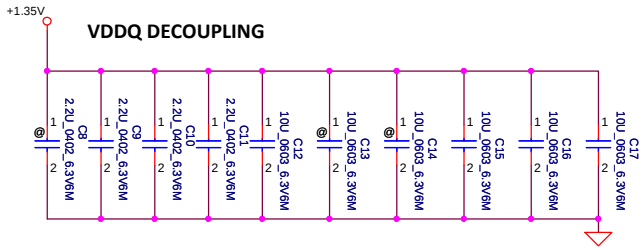
SVID DATA







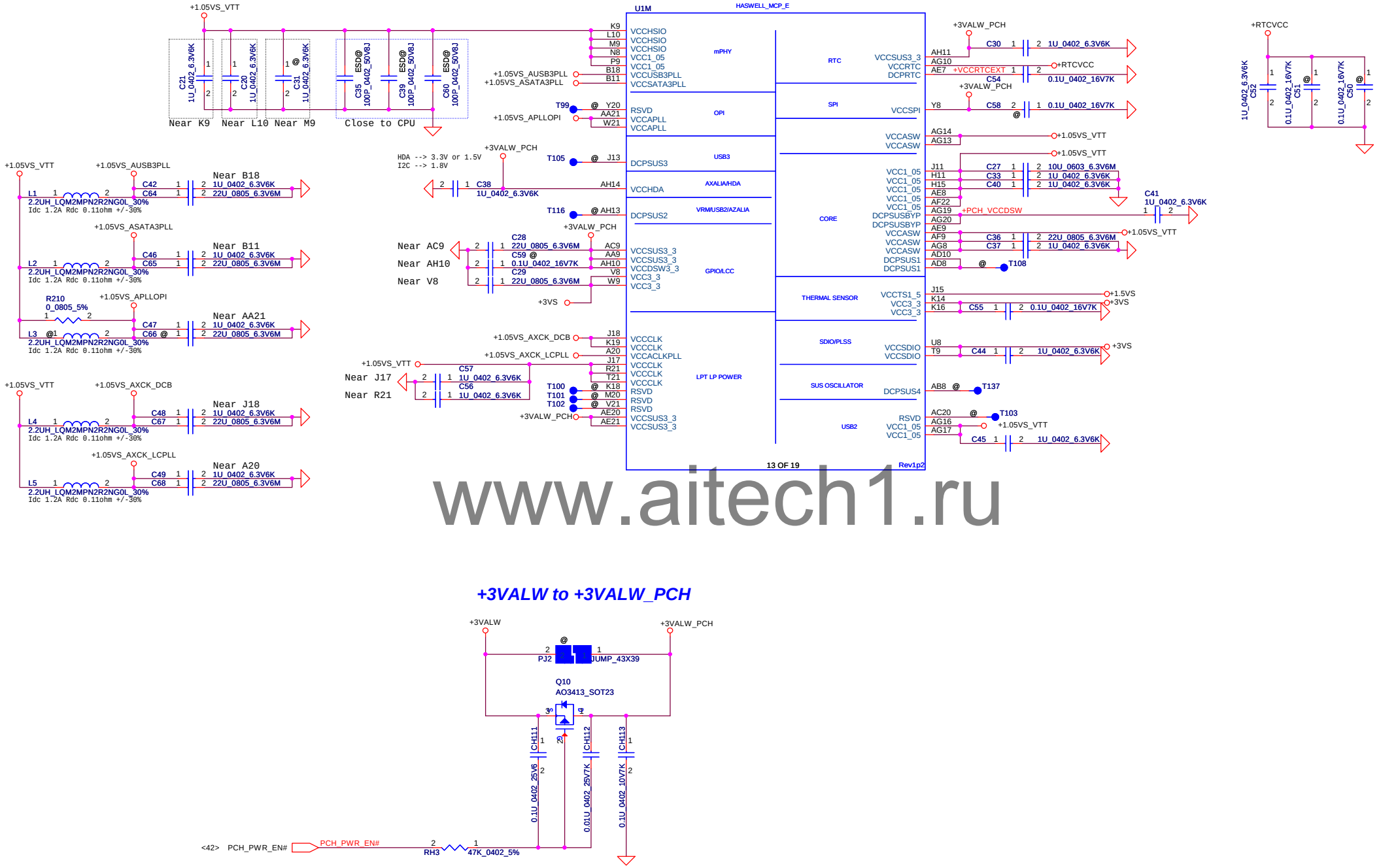
CC53 co-layout with C18



+1.35V : 470UF/2V/7343 *2
10UF/6.3V/0603 * 6
2.2UF/6.3V/0402 * 4

Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

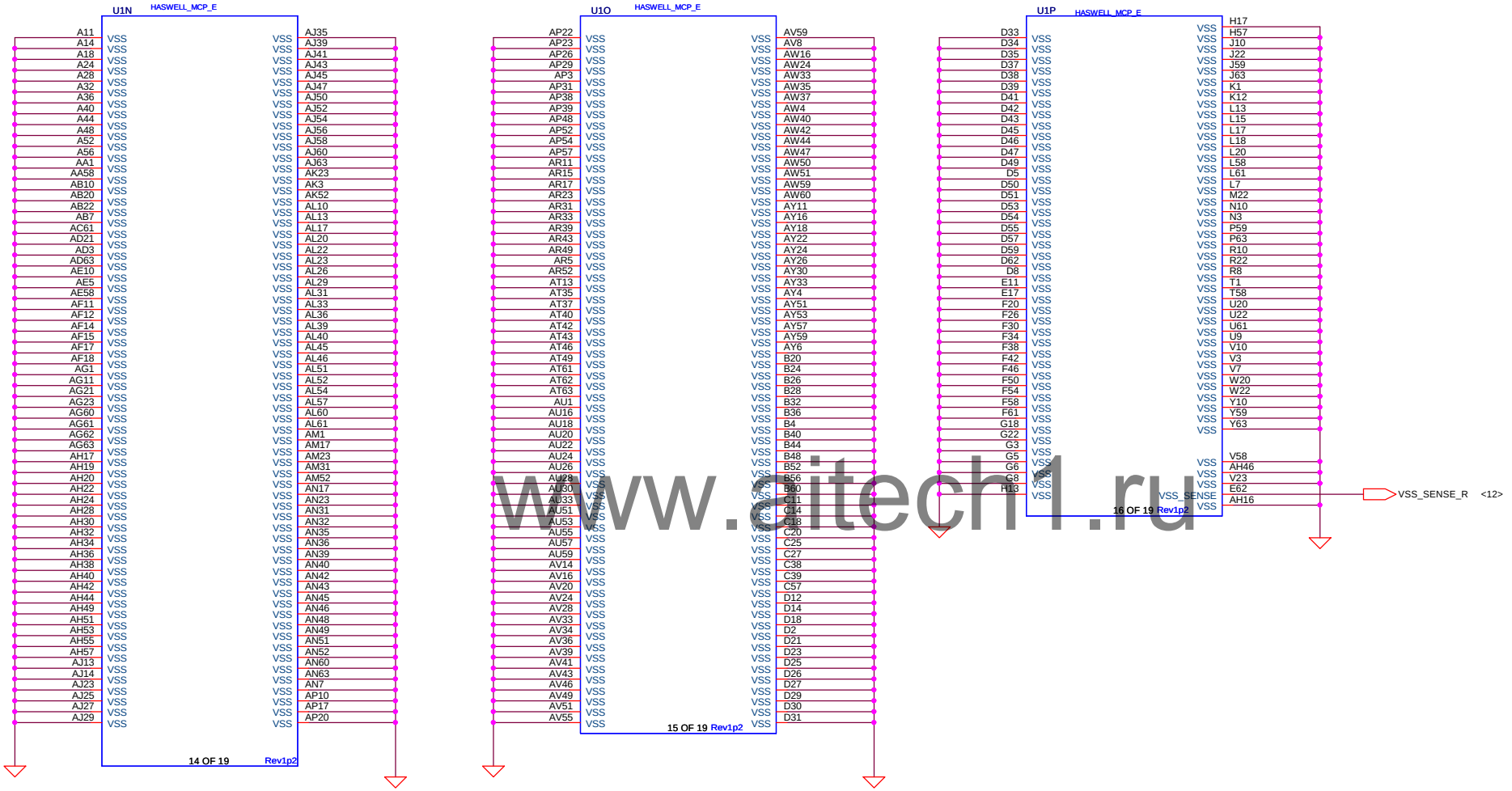
Compal Electronics, Inc.	
Title	HSW MCP(8/11) Power
Size: Custom	Document Number: VSKTA
Rev	1.0
Date: Tuesday, March 19, 2013	Sheet 12 of 53



+3VALW to +3VALW_PCH

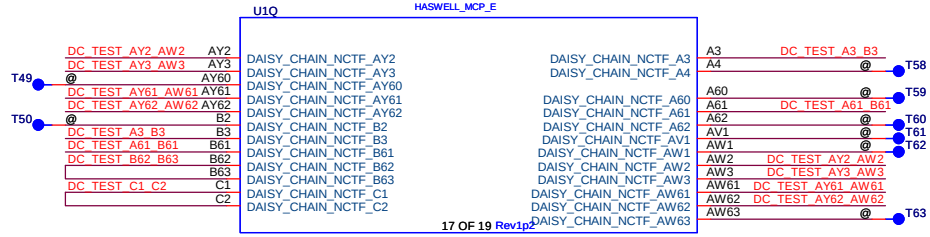
Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

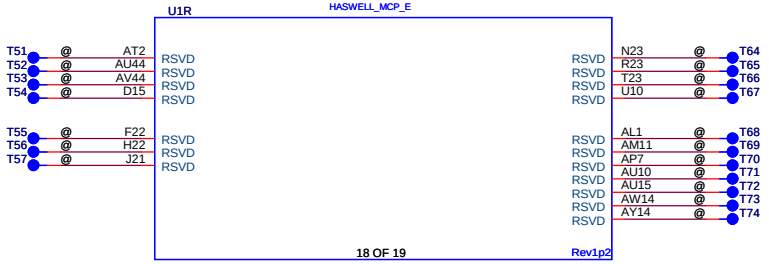
Compal Electronics, Inc.			
Title: HSW MCP(9/11) Power			
Size: Custom	Document Number: VSKTA		Rev: 1.0
Date: Tuesday, March 19, 2013	Sheet 13 of 53		

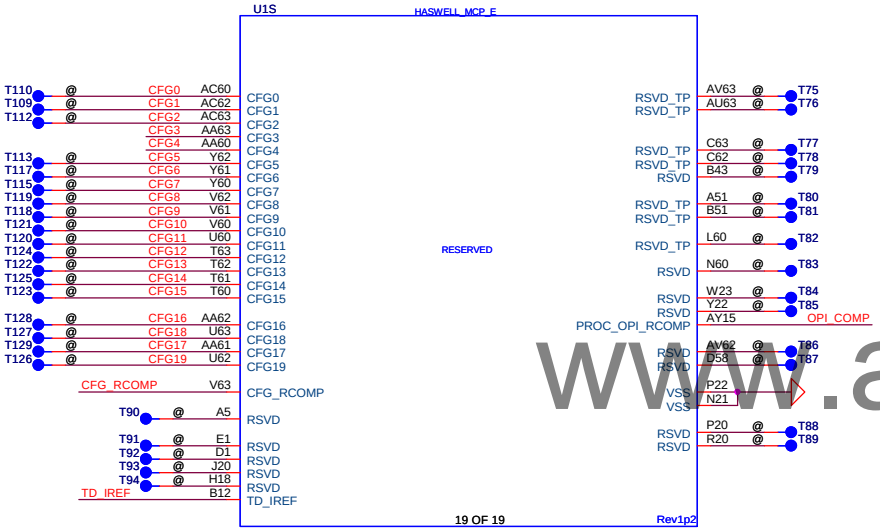


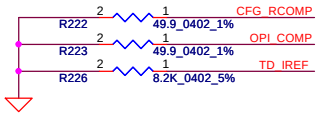
Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.	
Title	HSW MCP(10/11) GND
Size: Custom	Document Number: VSKTA
Rev	1.0
Date: Tuesday, March 19, 2013	Sheet 14 of 53

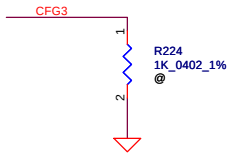




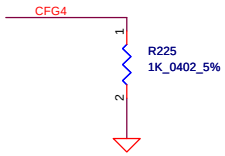




CFG Straps for Processor



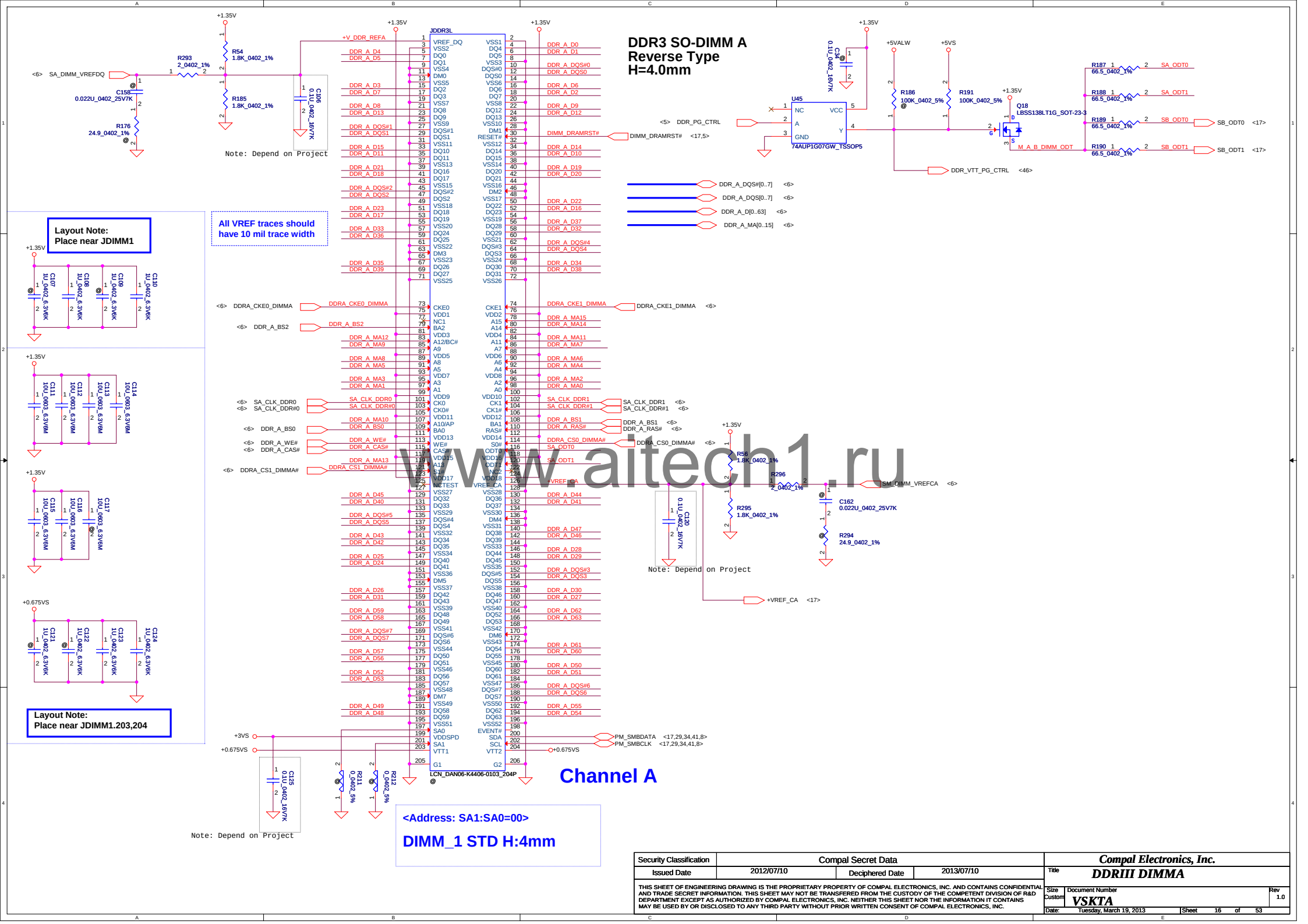
Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

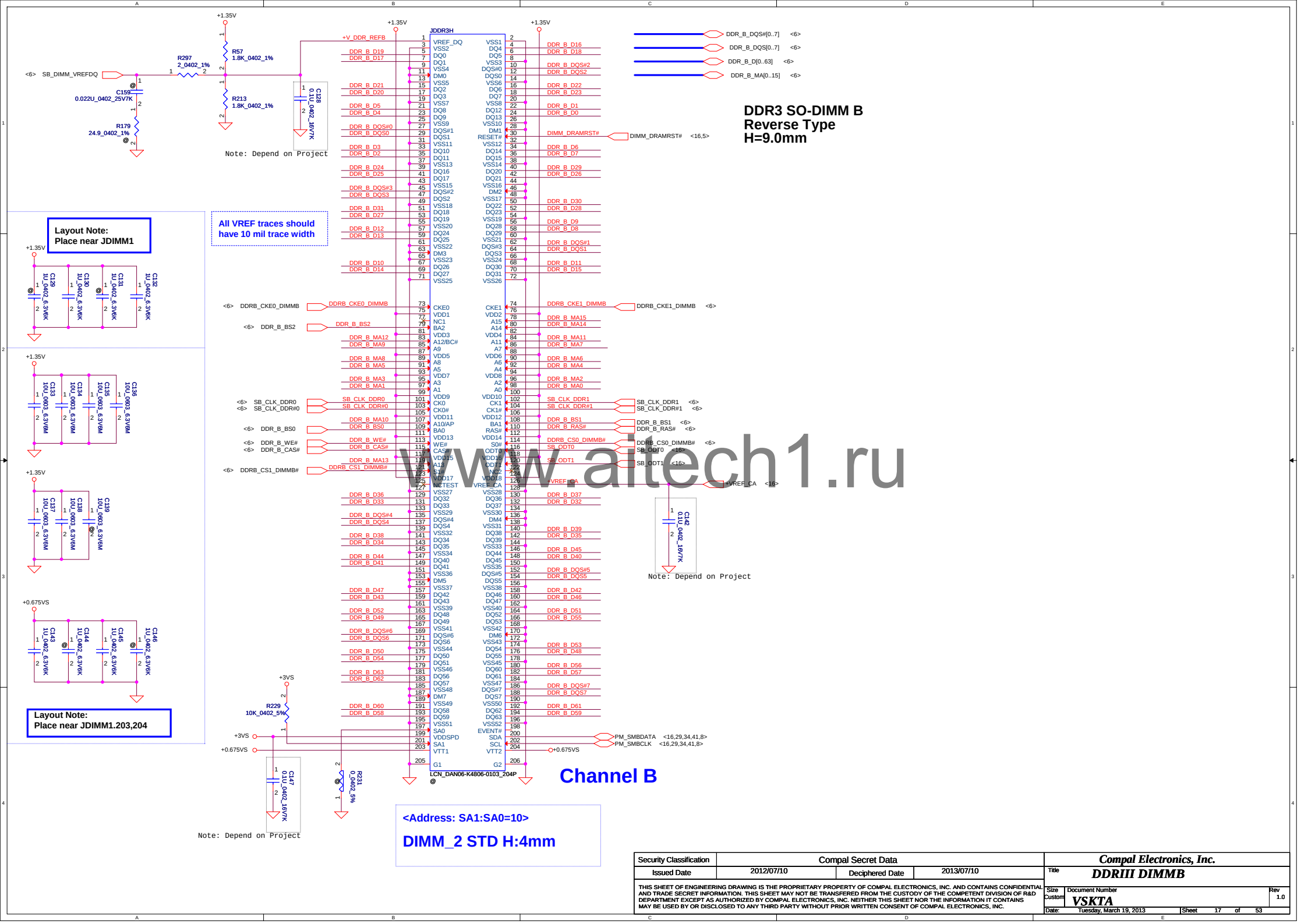
Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.			
Title	HSW MCP(11/11) RSVD		
Size: Custom	Document Number: VSKTA		Rev: 1.0
Date: Tuesday, March 19, 2013	Sheet 15 of 53		



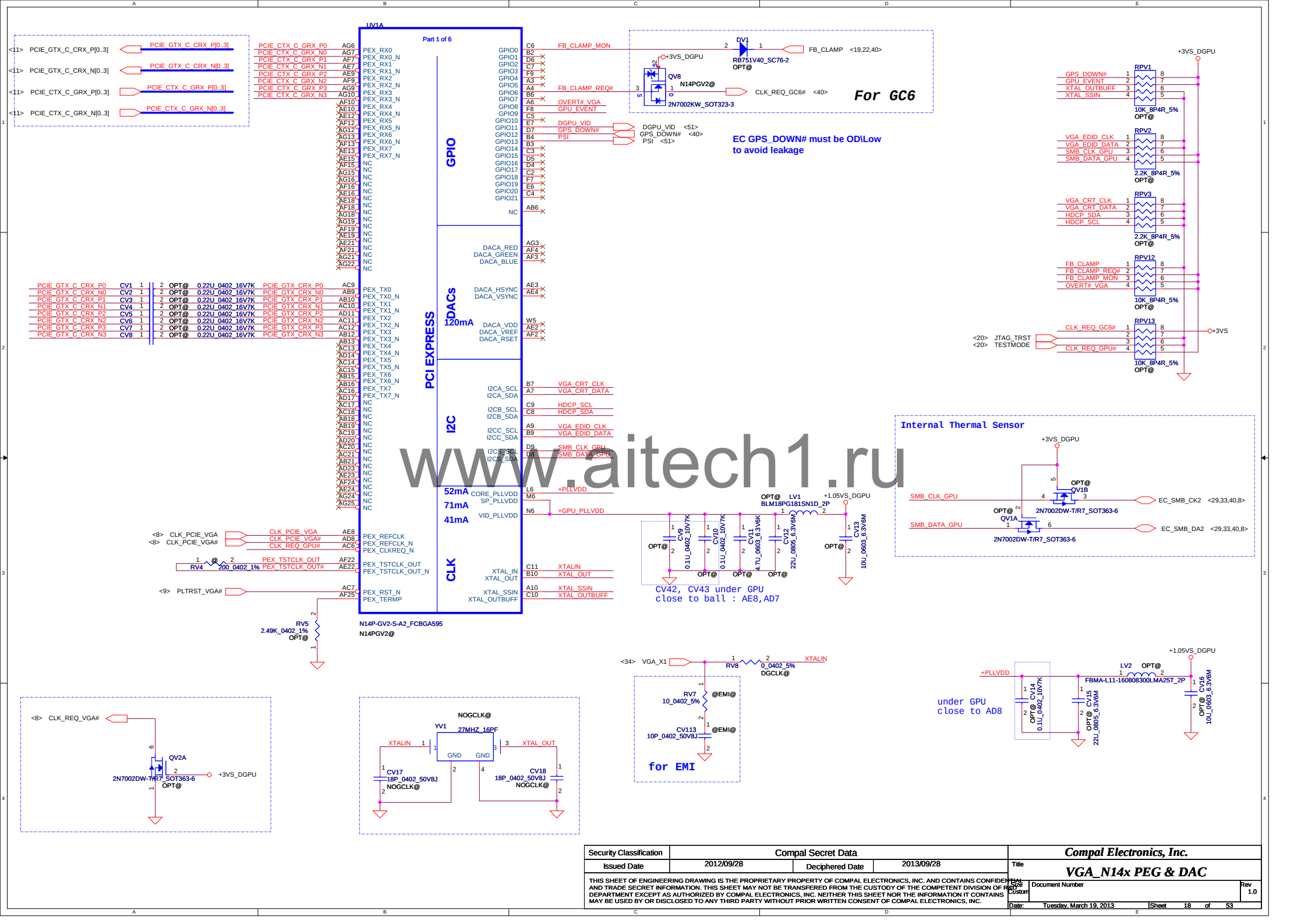
Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.			
Title: DDRIII DIMMA			
Size: Custom	Document Number: VSKTA		Rev: 1.0
Date: Tuesday, March 19, 2013	Sheet 16 of 53		



Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

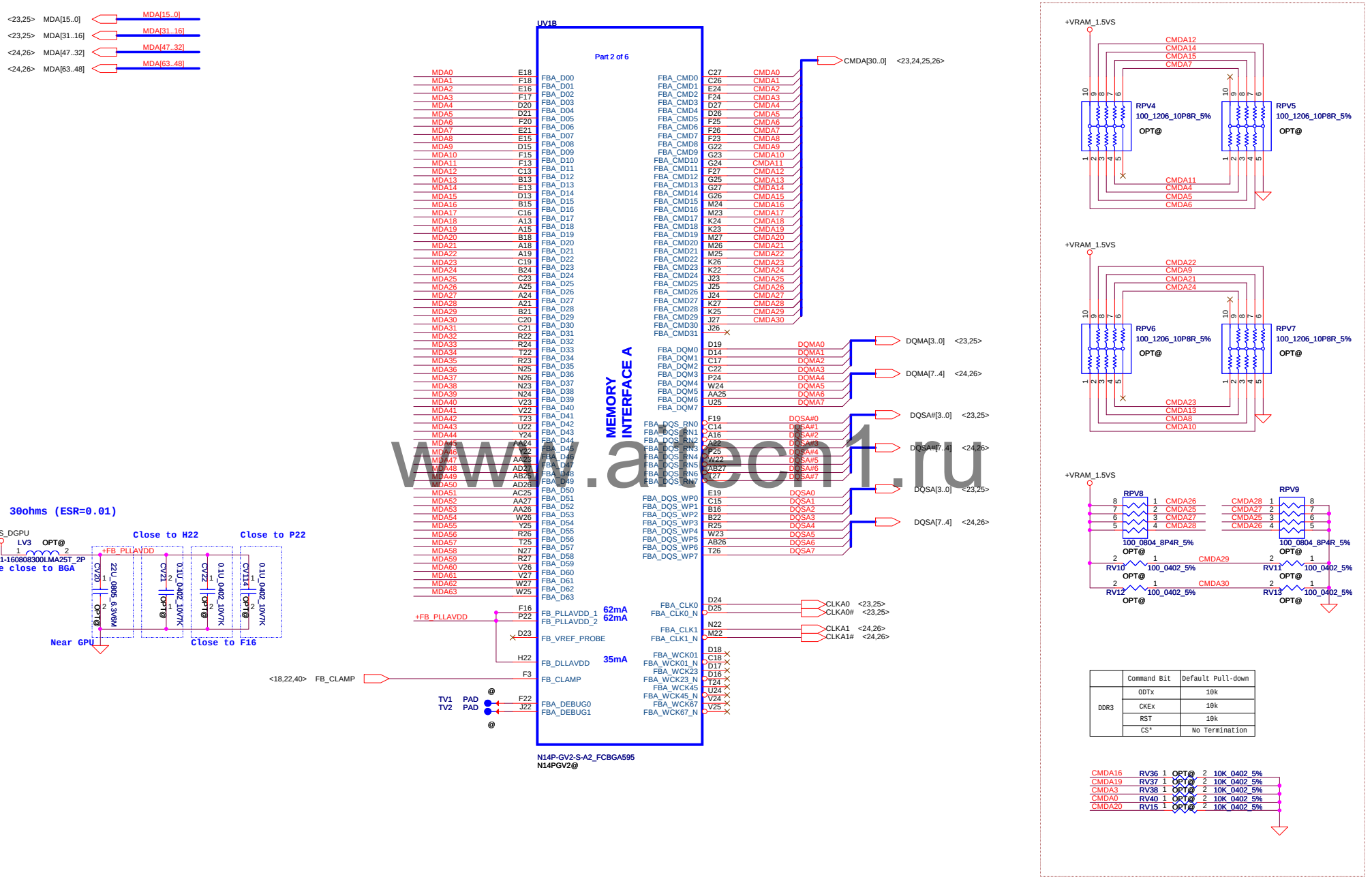
Compal Electronics, Inc.			
Title: DDRIII DIMMB			
Size: Custom	Document Number: VSKTA		Rev: 1.0
Date: Tuesday, March 19, 2013	Sheet 17 of 53		



Security Classification	Compal Secret Data		
Issued Date	2012/09/28	Deciphered Date	2013/09/28

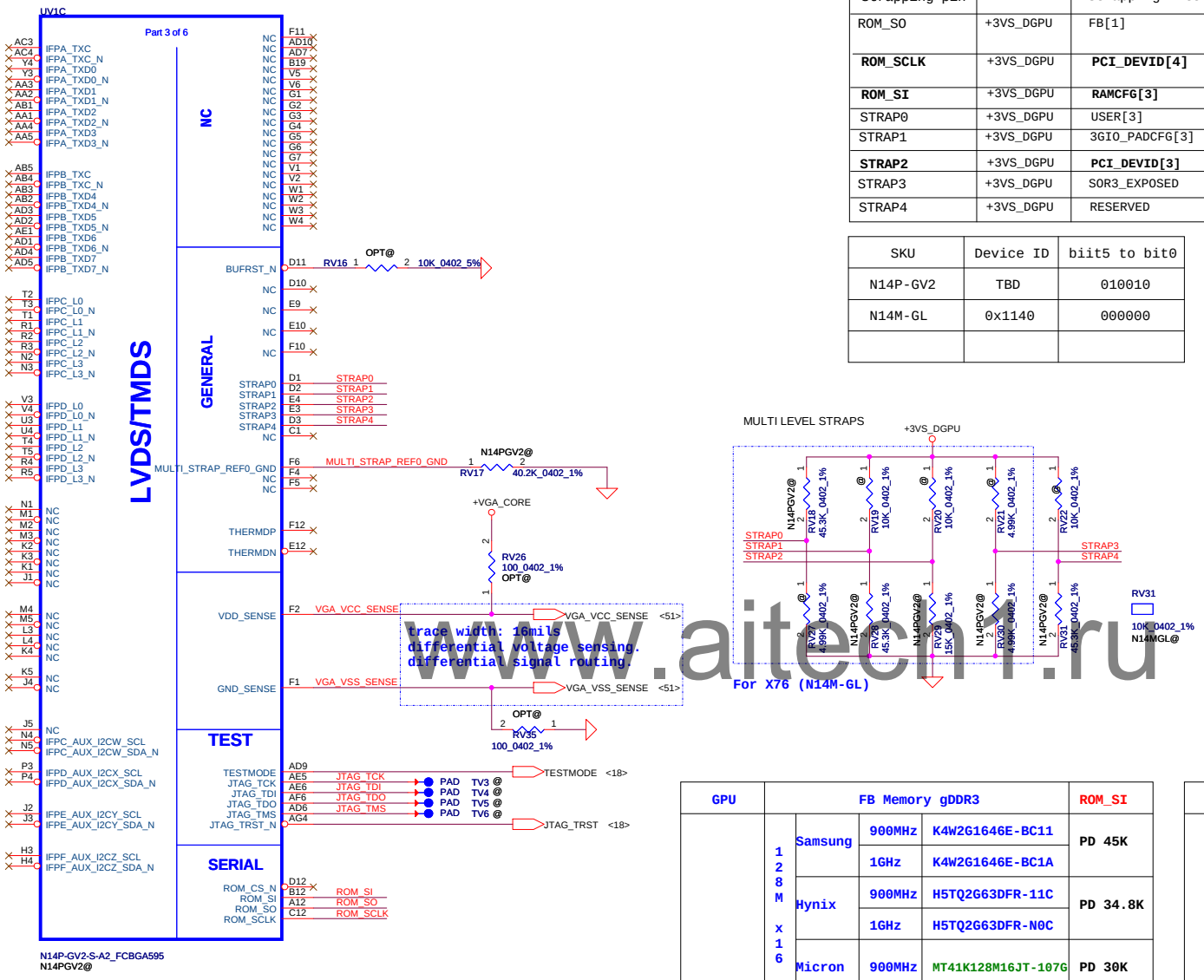
Compal Electronics, Inc.			
Title	VGA_N14x PEG & DAC		
Size	Document Number		Rev
Custom			1.0
Date:	Tuesday, March 19, 2013	Sheet	18 of 53

VRAM Interface



Security Classification	Compal Secret Data		
Issued Date	2012/09/28	Deciphered Date	2013/09/28

Compal Electronics, Inc.			
Title: N14x VRAM Interface			
Size: Custom	Document Number		Rev: 1.0
Date: Tuesday, March 19, 2013	Sheet 19 of 53		



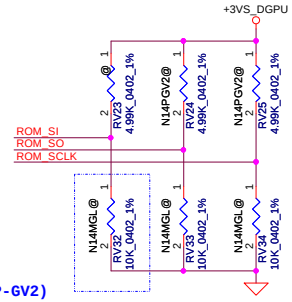
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	**PCI_DEVID[4]**	SUB_VENDOR	**PCI_DEVID[5]**	PEX_PLLEN_TERM
ROM_SI	+3VS_DGPU	**RAMCFG[3]**	**RAMCFG[2]**	**RAMCFG[1]**	**RAMCFG[0]**
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_DGPU	**PCI_DEVID[3]**	**PCI_DEVID[2]**	**PCI_DEVID[1]**	**PCI_DEVID[0]**
STRAP3	+3VS_DGPU	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_DGPU	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

SKU	Device ID	biit5 to bit0
N14P-GV2	TBD	010010
N14M-GL	0x1140	000000

Resistor Values	Pull-up to +3VS _DGPU	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

MULTI LEVEL STRAPS

For X76 (N14M-GL)



For X76 (N14P-GV2)

trace width: 16mils
differential voltage sensing.
differential signal routing.

GPU		FB Memory gDDR3			ROM_SI
N14P-GV2	128M x 16	Samsung	900MHz	K4W2G1646E-BC11	PD 45K
			1GHz	K4W2G1646E-BC1A	
		Hynix	900MHz	H5TQ2G63DFR-11C	PD 34.8K
			1GHz	H5TQ2G63DFR-N0C	
		Micron	900MHz	MT41K128M16JT-107G	PD 30K
	256M x 16	Samsung	900MHz	K4W4G1646B-HC11	PD 20K
		Micron	900MHz	MT41K256M16HA-107G	PD 10K

GPU		FB Memory gDDR3			STRAP[3:0]
N14M-GL	128M x 16	Samsung	900MHz	K4W2G1646E-BC11	0101
			1GHz	K4W2G1646E-BC1A	
		Hynix	900MHz	H5TQ2G63DFR-11C	0110
			1GHz	H5TQ2G63DFR-N0C	
		Micron	900MHz	MT41K128M16JT-107G	0001
	256M x 16	Samsung	900MHz	K4W4G1646B-HC11	1011
		Hynix	900MHz	H5TC4G63AFR-11C	0100
		Micron	900MHz	MT41K256M16HA-107G	1101

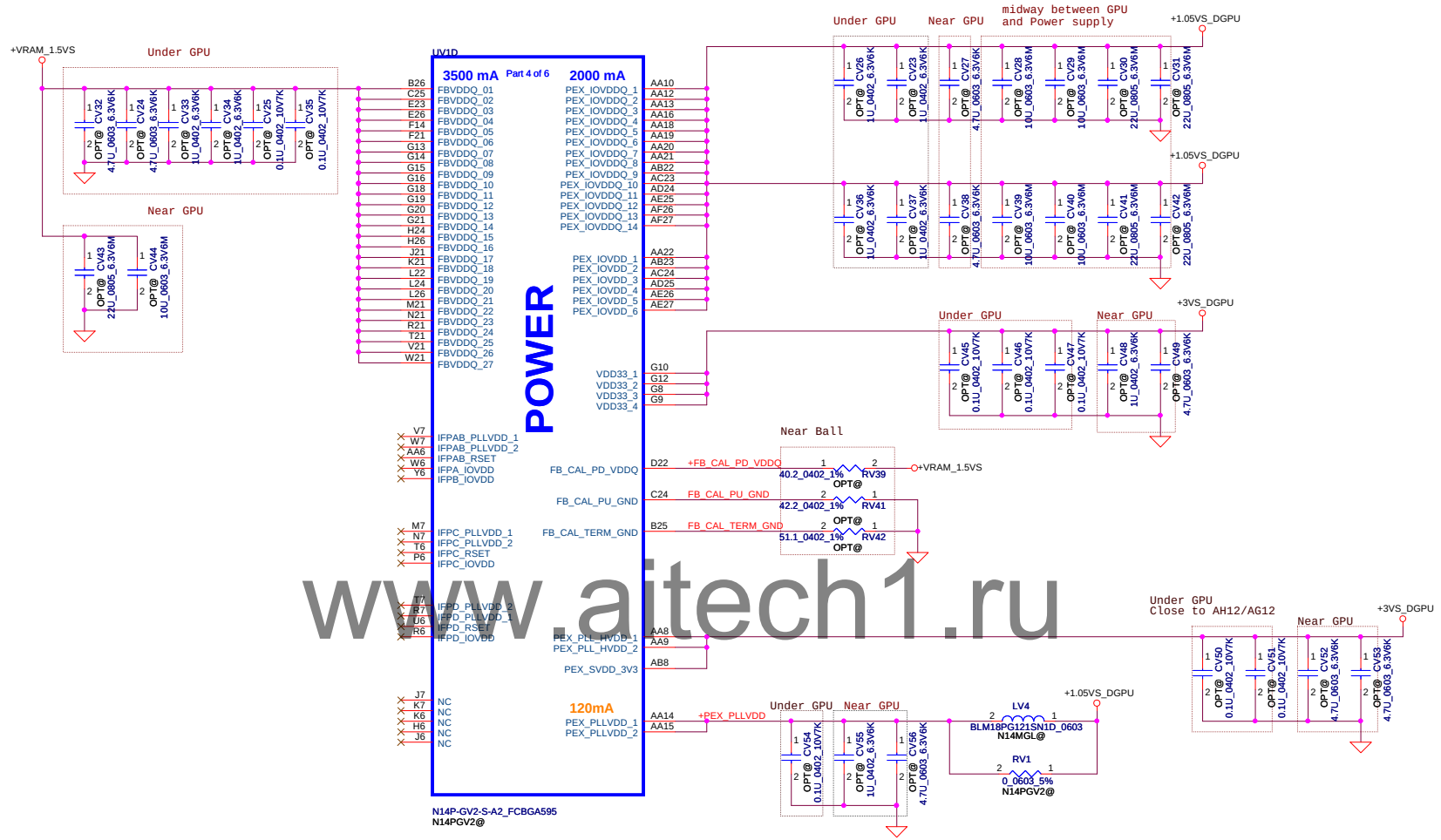
Security Classification	Compal Secret Data		
Issued Date	2012/09/28	Deciphered Date	2013/09/28

Compal Electronics, Inc.

Title: VGA_N14x LVDS&TMDS

Size: Custom | Document Number | Rev 1.0

Date: Tuesday, March 19, 2013 | Sheet 20 of 53



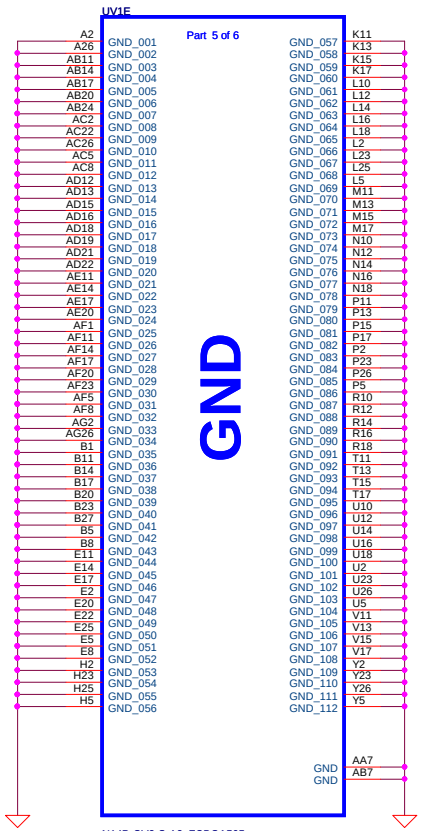
Security Classification	Compal Secret Data		
Issued Date	2012/09/28	Deciphered Date	2013/09/28

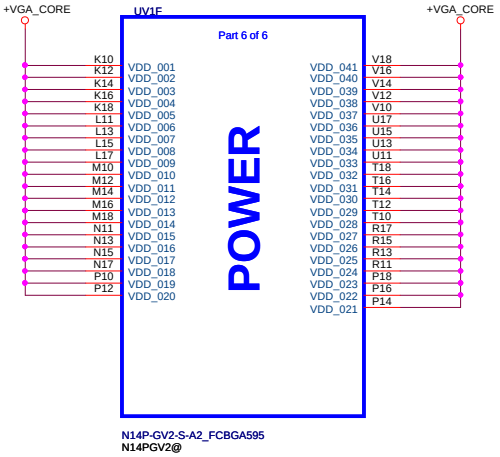
Compal Electronics, Inc.

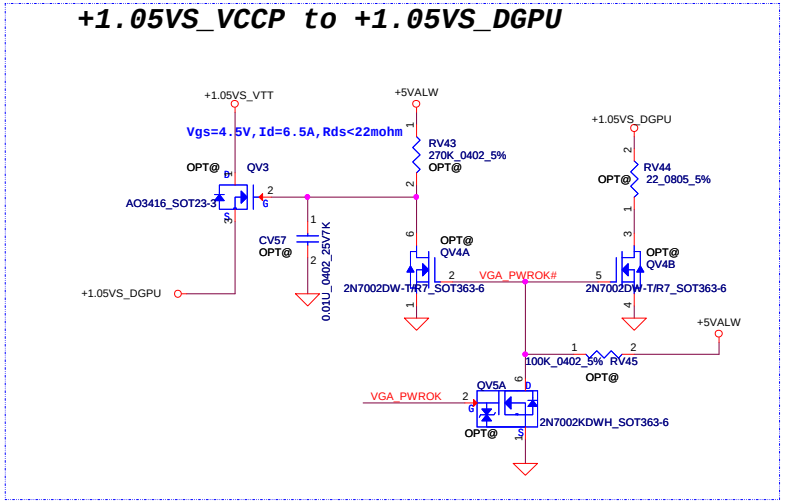
Title: **VGA_N14x POWER**

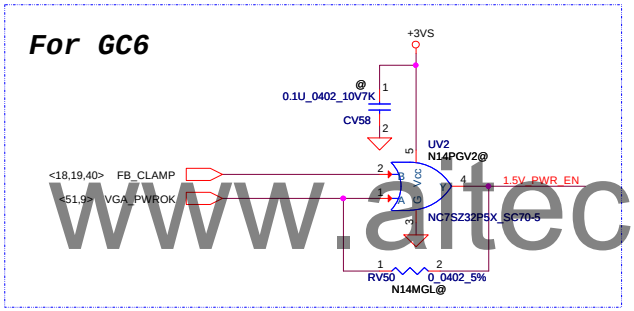
Size	Document Number	Rev
Custom		1.0

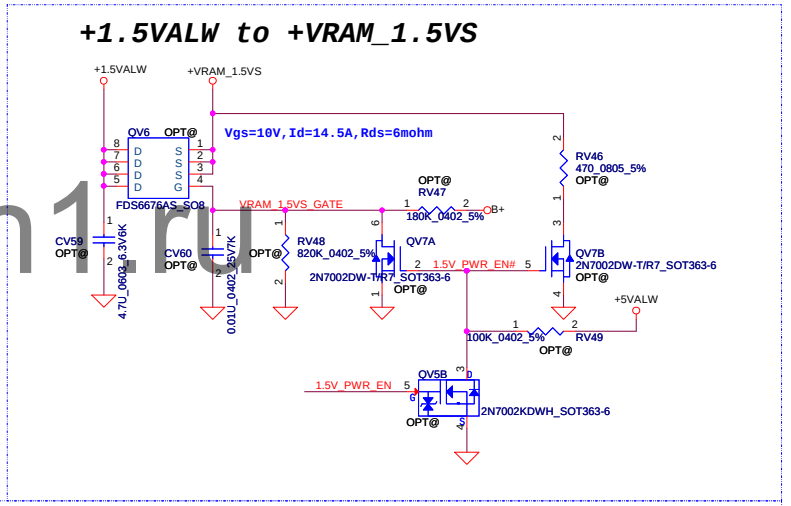
Date: Tuesday, March 19, 2013 Sheet 21 of 53

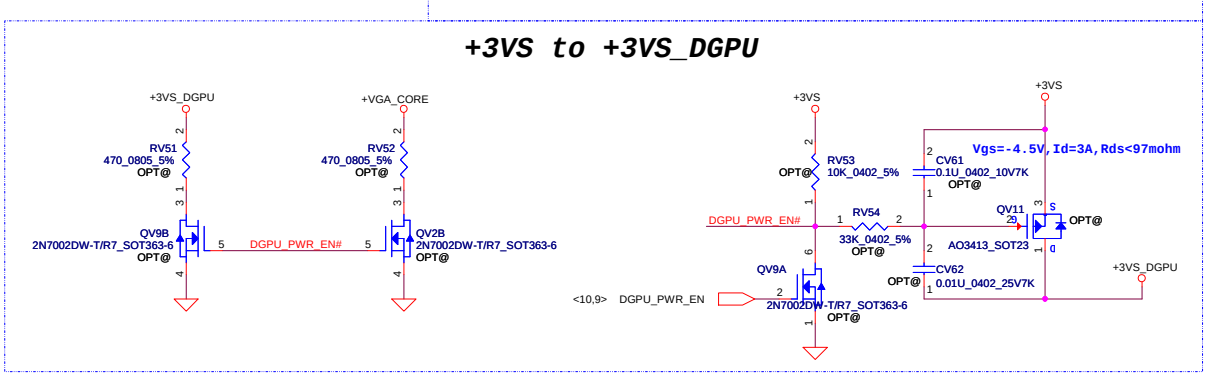












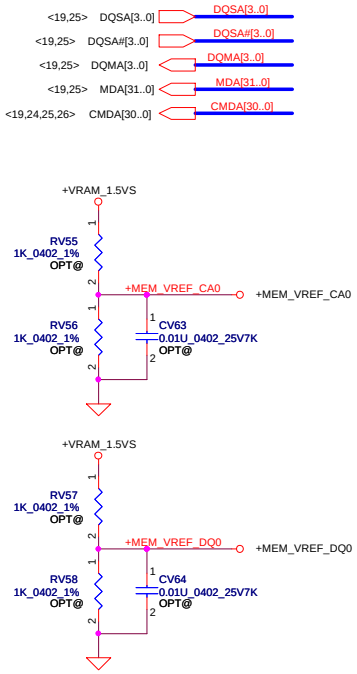
Security Classification	Compal Secret Data		
Issued Date	2012/09/28	Deciphered Date	2013/09/28

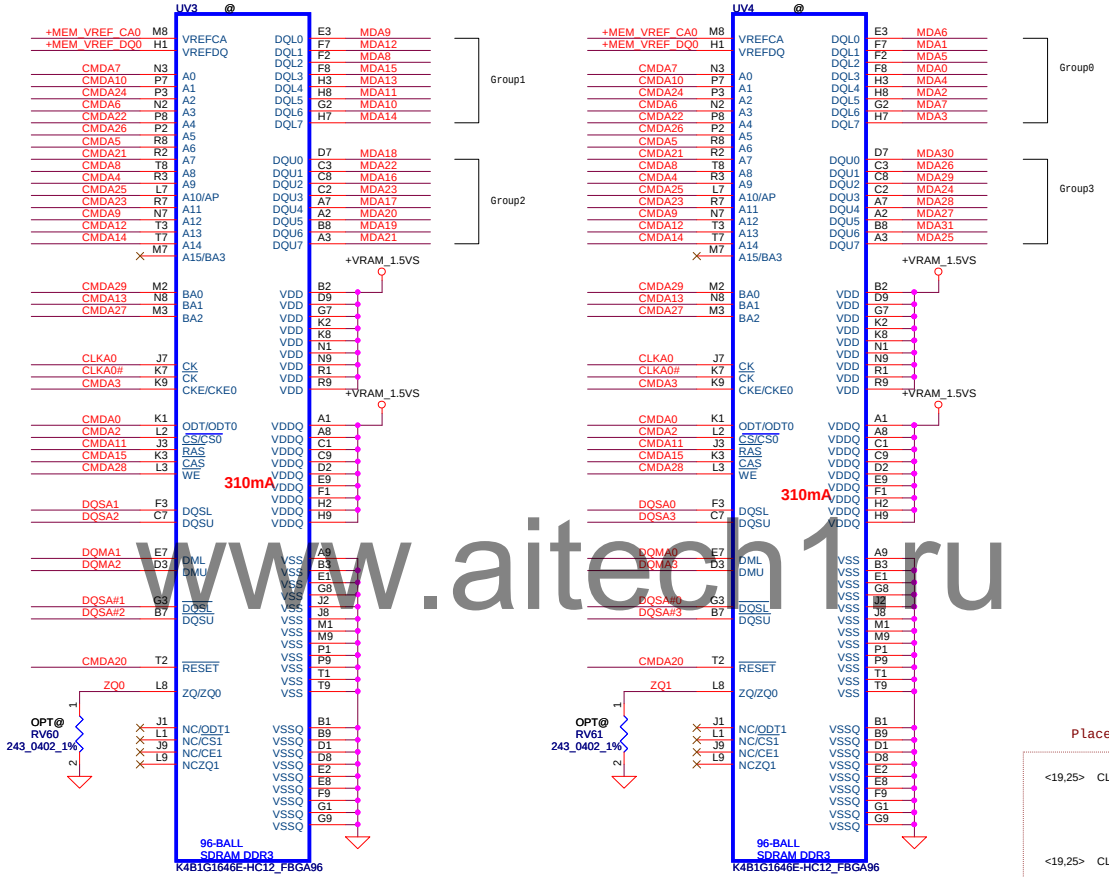
Compal Electronics, Inc.	
Title	VGA_N14x POWER & GND
Size: Custom	Document Number
Rev	1.0
Date: Tuesday, March 19, 2013	Sheet 22 of 53

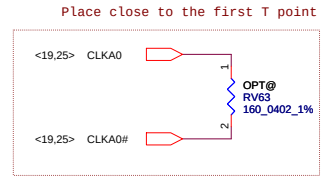
RANK 0 [31...0]

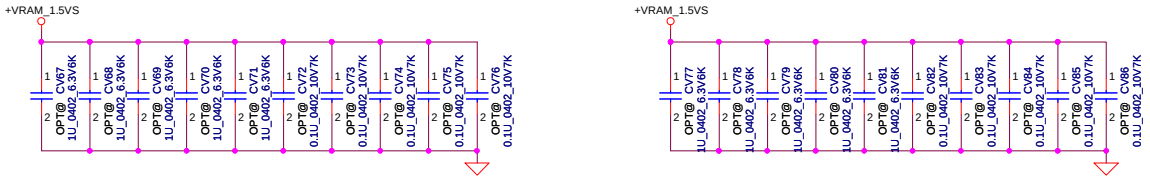
VRAM DDR3 Chips

Mode E Address	Rank 0 0..31	Rank 0 32..63	Rank 1 0..31	Rank 1 32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2









Security Classification	Compal Secret Data		
Issued Date	2012/09/28	Deciphered Date	2013/09/28

Compal Electronics, Inc.

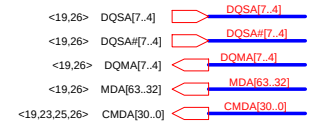
Title: **VGA_N14x VRAM RANK 0L**

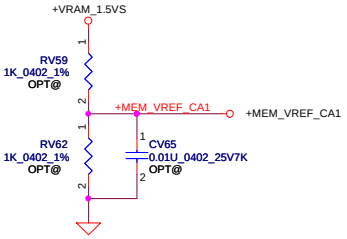
Size	Document Number	Rev
Custom		1.0

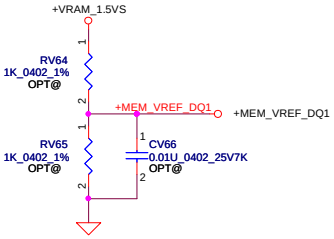
Date: Tuesday, March 19, 2013 Sheet 23 of 53

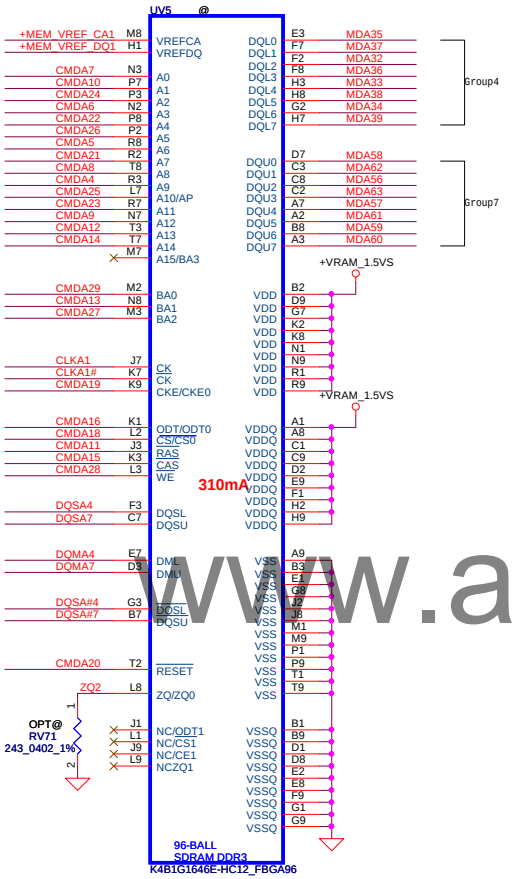
RANK 0 [63...32]

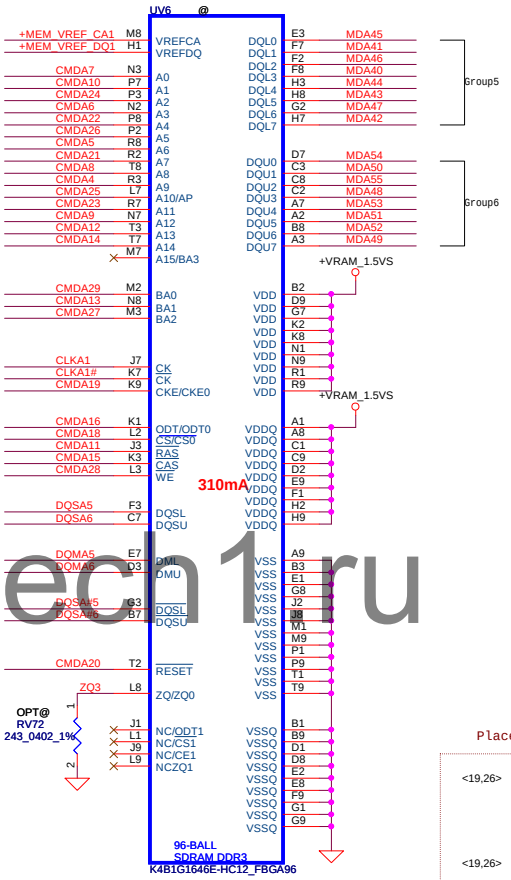
VRAM DDR3 Chips





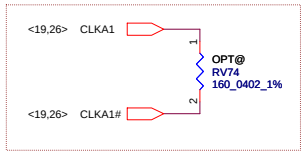


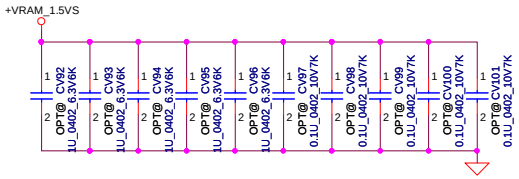


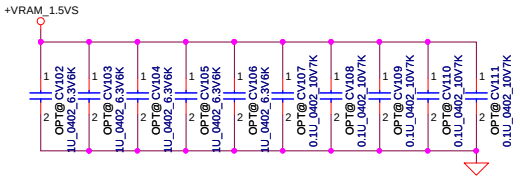


Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

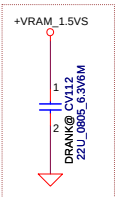
Place close to the first T point







Place close to RANK1 VRAM



Security Classification	Compal Secret Data		
Issued Date	2012/09/28	Deciphered Date	2013/09/28

Compal Electronics, Inc.

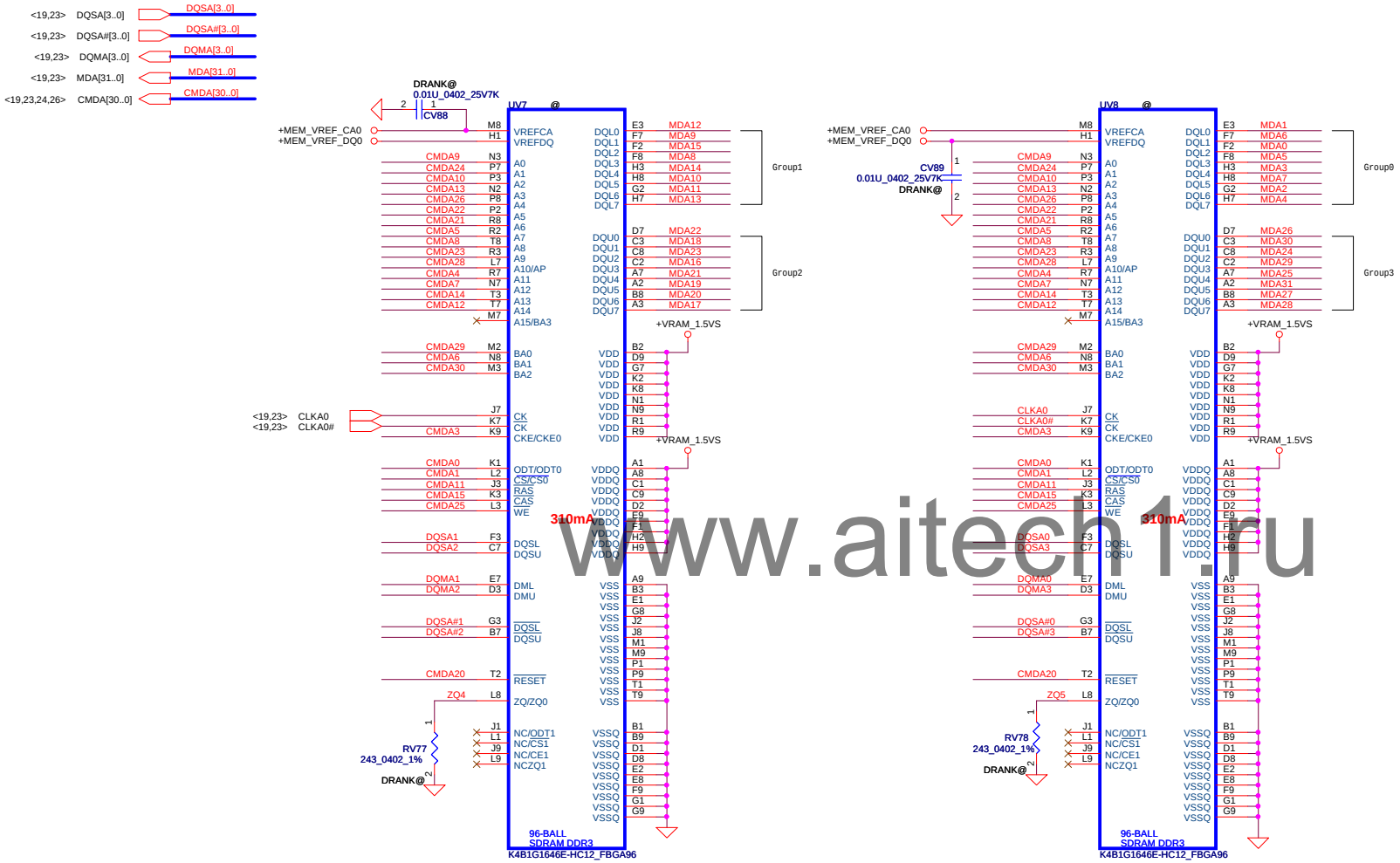
Title: VGA_N14x VRAM RANK 0H

Size	Document Number	Rev
Custom		1.0

Date: Tuesday, March 19, 2013 Sheet 24 of 53

RANK 1 [31...0]

VRAM DDR3 Chips



Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

Security Classification	Compal Secret Data		
Issued Date	2012/09/28	Deciphered Date	2013/09/28

Compal Electronics, Inc.

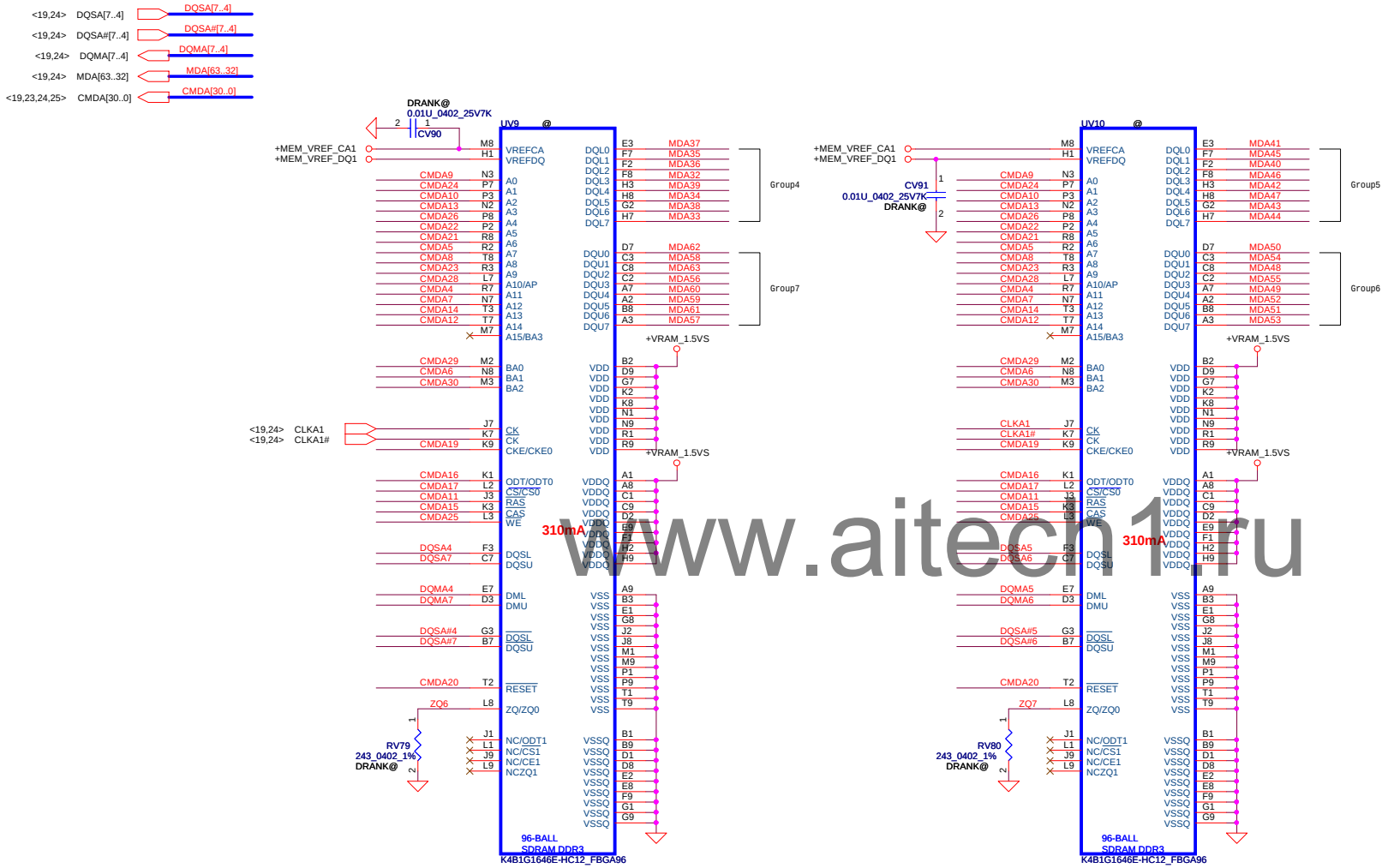
Title: VGA_N14x VRAM RANK 1L

Size: Custom | Document Number | Rev: 1.0

Date: Tuesday, March 19, 2013 | Sheet 25 of 53

RANK 1 [63...32]

VRAM DDR3 Chips



Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

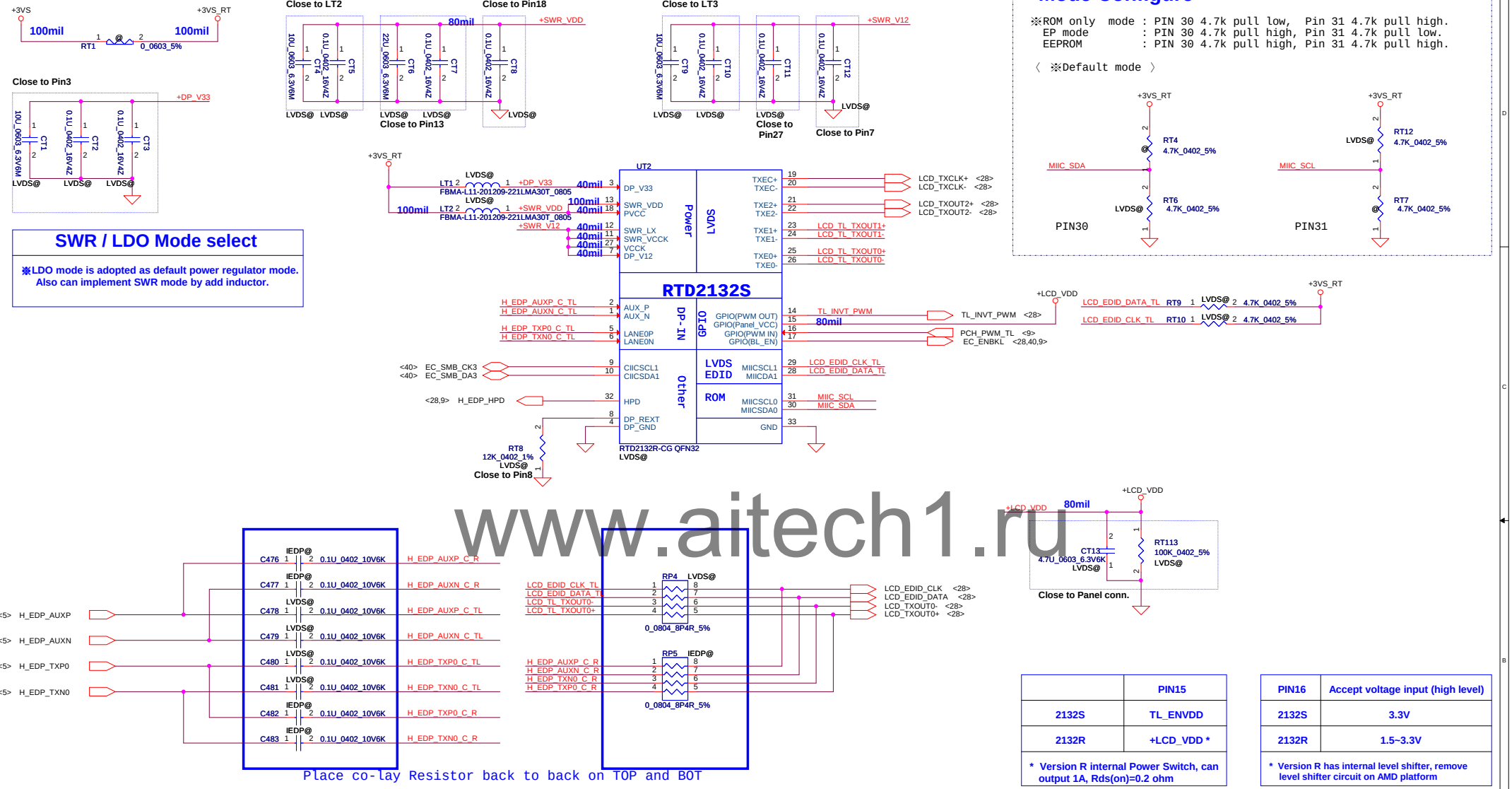
Security Classification	Compal Secret Data		
Issued Date	2012/09/28	Deciphered Date	2013/09/28

Compal Electronics, Inc.

Title: VGA_N14x VRAM RANK 1H

Size	Document Number	Rev
Custom		1.0

Date: Tuesday, March 19, 2013 Sheet 26 of 53



	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *

* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

PIN16	Accept voltage input (high level)
2132S	3.3V
2132R	1.5~3.3V

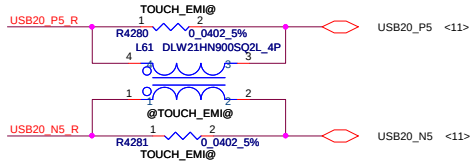
* Version R has internal level shifter, remove level shifter circuit on AMD platform

Different between 2132S and 2132R

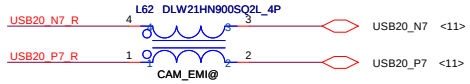
2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/30	Deciphered Date 2013/06/30	Title: LVDS Translator - RTD2132S
			Size: Custom; Document Number: VSKAA; Rev: 1.0
			Date: Tuesday, March 19, 2013; Sheet 27 of 53

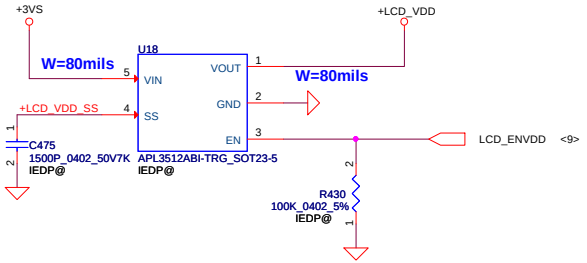
BTO : TOUCH_EMI@



EMI request - Close to JEDP connector

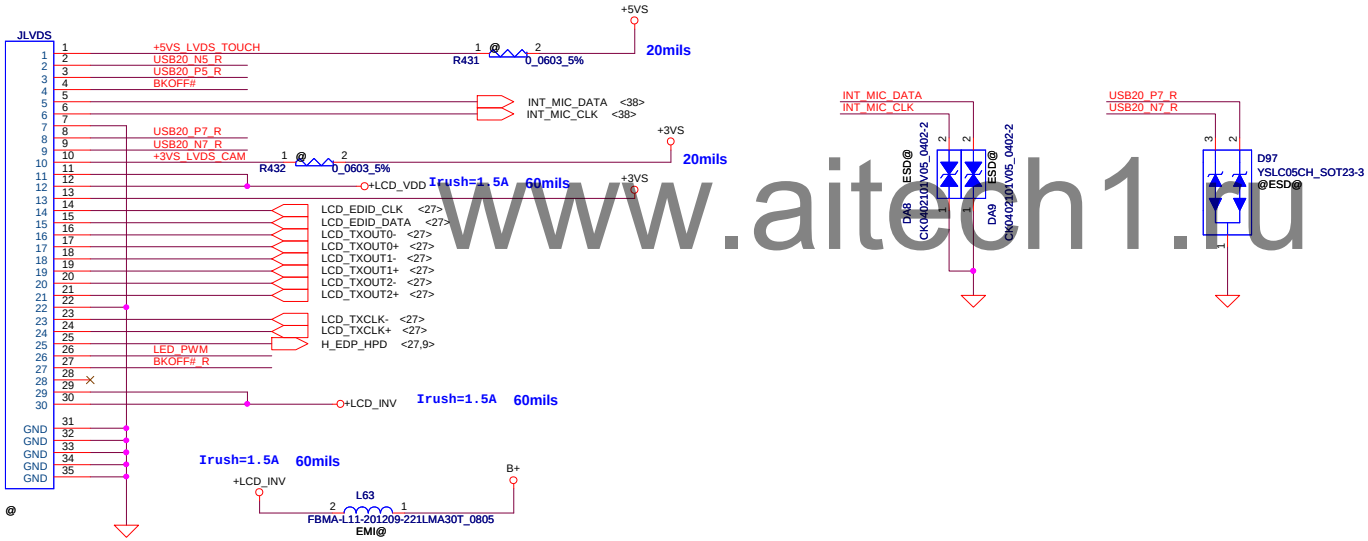


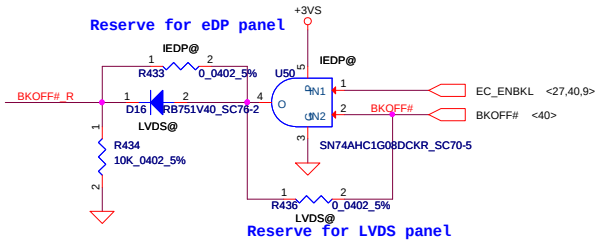
LCD POWER CIRCUIT (For EDP panel only)

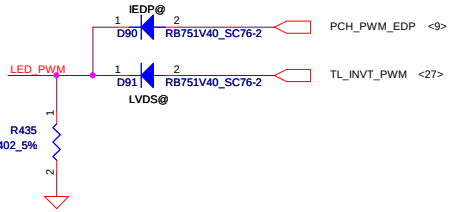


LVDS colay eDP cable

Pin define will be change after ME ready







Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: LVDS

Size: D26 Custom	Document Number: VSKTA		Rev: 1.0
Date: Tuesday, March 19, 2013	Sheet 28 of 53		

Default to PS8401 & PS8201 I2C Control Mode

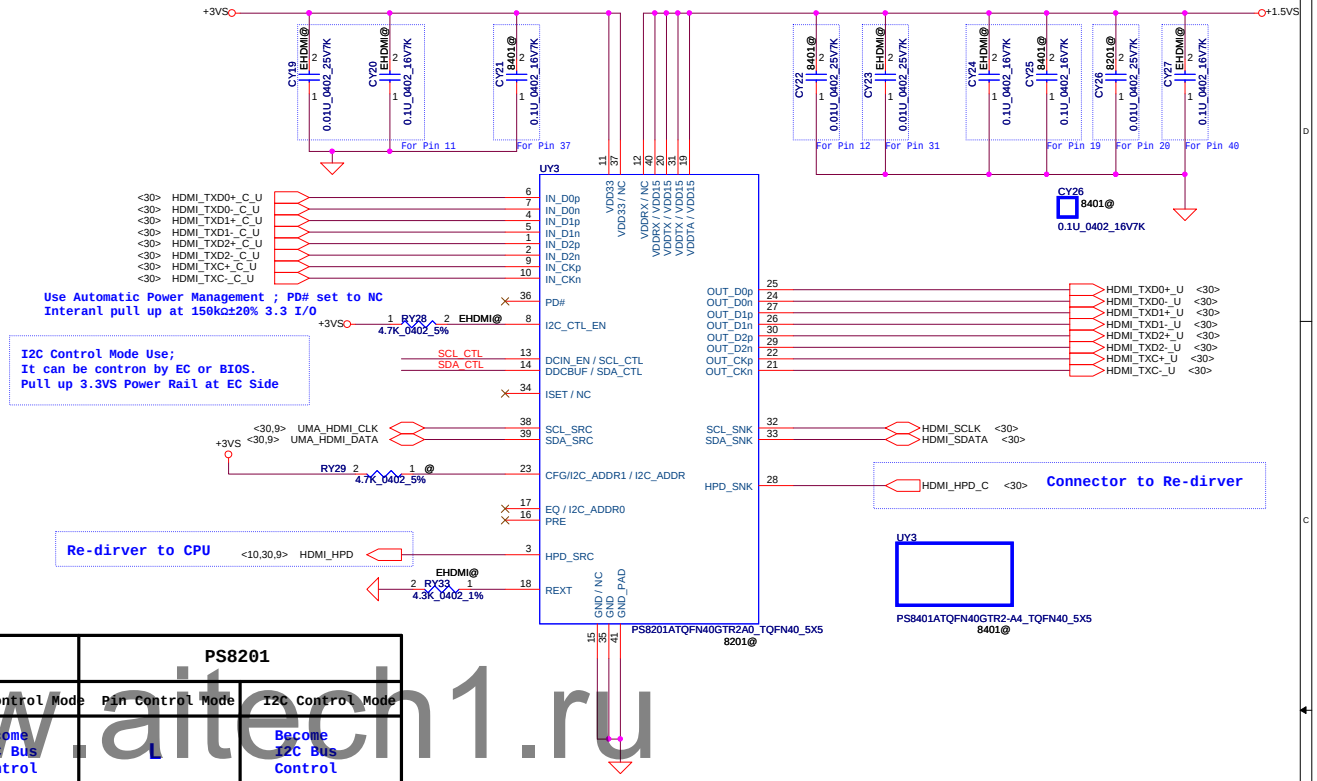
I2C Mode HDMI ID Setting

If PS8401 use I2C Mode , EQ=I2C_ADDR0 , CFG = I2C_ADDR1

For PS8401
I2C control bus address LSB; Internal pull down at 150kohz±20%, 3.3V I/O.
[I2C_ADDR1, I2C_ADDR0] ; I2C Address (W/R)=
LL: 0x4C/4D (default)
LH: 0x5C/5D
HL: 0xCC/CD
HH: 0xEC/ED

If PS8401 use I2C Mode , EQ=I2C_ADDR

For PS8201
I2C control bus address LSB; Internal pull down at ~150k ohz, 3.3V I/O.
[I2C_ADDR] ; I2C Address (W/R)=
L: 0x64/65 (default)
H: 0xE4/E5



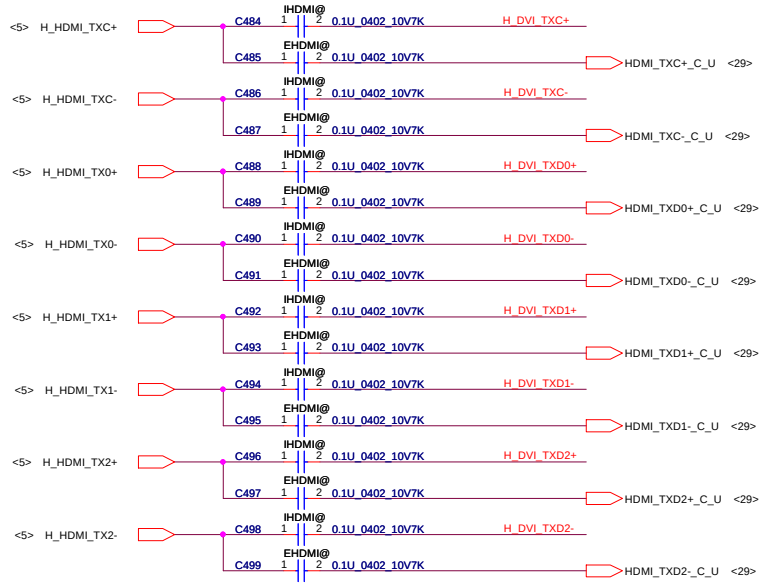
Strap H:3.3V M:1.65V L:0V

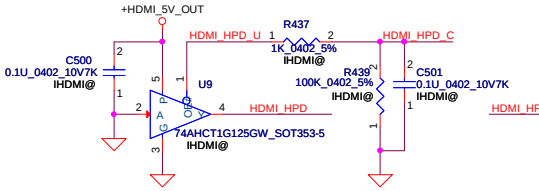
Net name	Description	PS8401		PS8201	
		Pin Control Mode	I2C Control Mode	Pin Control Mode	I2C Control Mode
DCIN_EN	DC cou;ing enable; Internal pull down at 150k ohz ±20%, 3.3V I/O. L: default, AC coupling input H: DC coupling input	L	Become I2C Bus Control	L	Become I2C Bus Control
DDCBUF	Enable active DDC buffer; Internal pull down at 150k?±20%, 3.3V I/O. L: default, passive DDC pass-through H: active DDC buffer with default threshold M: active DDC buffer without internal pull up resistor	M	Become I2C Bus Control	M	Become I2C Bus Control
ISET	TMDS output swing adjustment; Internal pull down at 150kΩ±20%, 3.3V I/O. For PS8401 Only ISET = L: Default H: Increase +13% M: Reduce -13%	L	NC	NC	NC
CFG	CFG: Configuration pin, 3.3V IO, internal pull down at 150kΩ±20%. 3.3V I/O CFG = L: HDMI ID disable H: HDMI ID enable	H	NC	H	NC
EQ	EQ:Receiver equalization setting;; Internal pull down at ~150k?, 3.3V I/O For PS801 EQ = L:programmable EQ for channel loss up to 6.5dB @ 3.0Gbps H:programmable EQ for channel loss up to 9.5dB @ 3.0Gbps M:programmable EQ for channel loss up to 3dB @ 3.0Gbps For PS8401 EQ = L:programmable EQ for channel loss up to 12.4dB H:programmable EQ for channel loss up to 4.3dB M:programmable EQ for channel loss up to 8.6dB	M	NC	M	NC
PRE	Output pre-emphasis setting; Internal pull down at 150kΩ±20%, 3.3V I/O. PRE = L: No pre-emphasis H: 1.6dB pre-emphasis M: 2.5dB pre-emphasis	L	NC	L	NC
I2C_CTL_EN	I2C Control enable. Internal pull down at 150kΩ±20%. 3.3V I/O I2C_CTL_EN = LOW (L): Pin Control is selected. HIGH (H): I2C Control is selected.	L	H	L	H

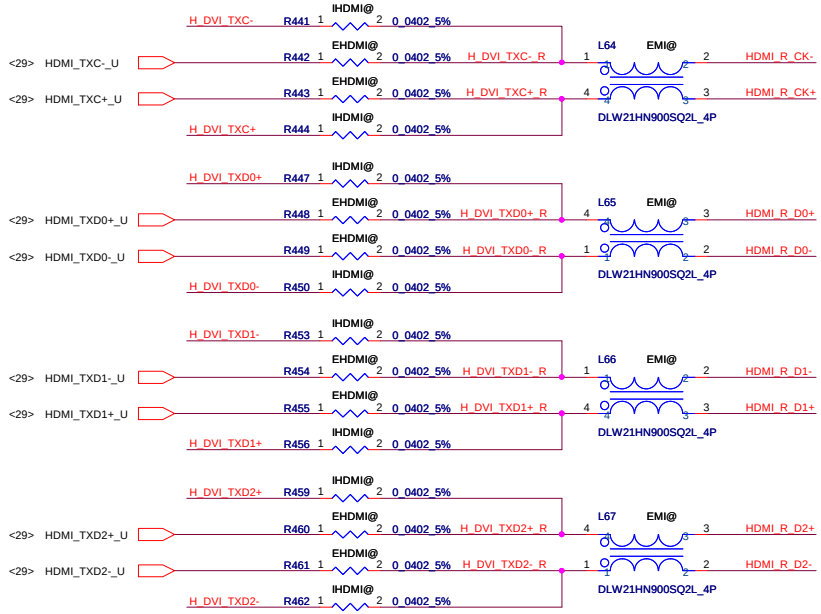
Note: PS8401 have Jitter cleaning function and can control TMDS output swing , PS8201 don't have.

Security Classification	Compal Secret Data		
Issued Date	2012/??/??	Deciphered Date	2015/??/??

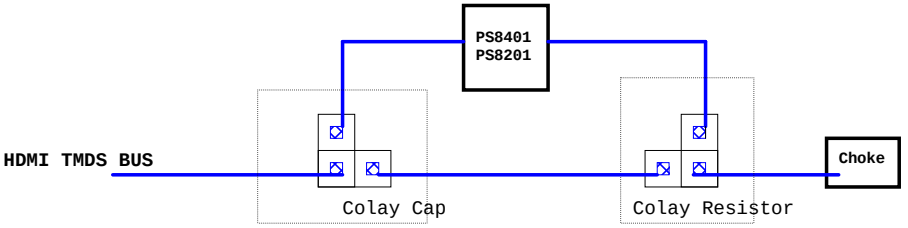
Compal Electronics, Inc.			
Title	HDMI Re-driver		
Size	Document Number	PS8201A & PS8401A	Rev 1.0
Date: Tuesday, March 19, 2013	Sheet 29 of 53		





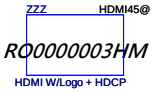


Common CHOKE use 67ohm



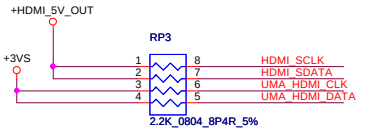
Componet close to Conn.
Impedance depend on platform design guide

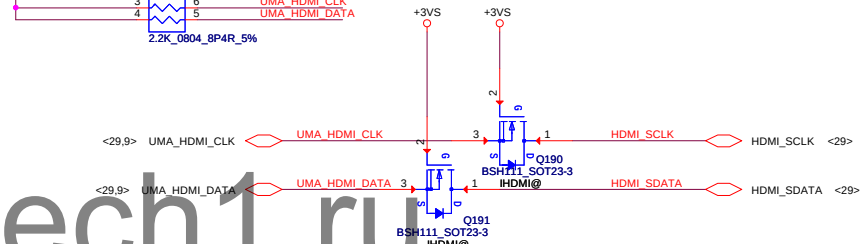
HDMI Royalty



HDMI W/O Logo: RO0000001HM
HDMI W/Logo: RO0000002HM
HDMI W/Logo + HDCP: RO0000003HM

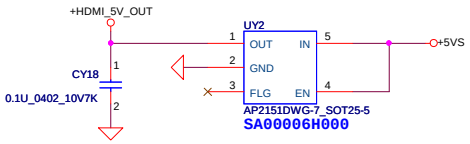
please manually load
this virtual material to 45@ BOM

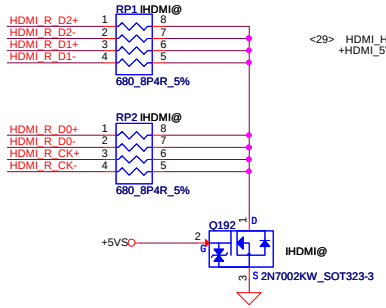




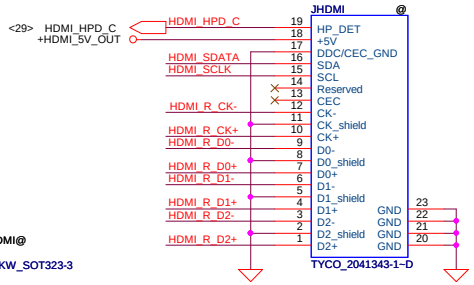
HDMI POWER CIRCUIT

VIN = 5V, IOUT = 0.5A , RDS(ON) TYP=95m ; MAX=115m
Current Limit: TYP=0.8A ; MAX=1A



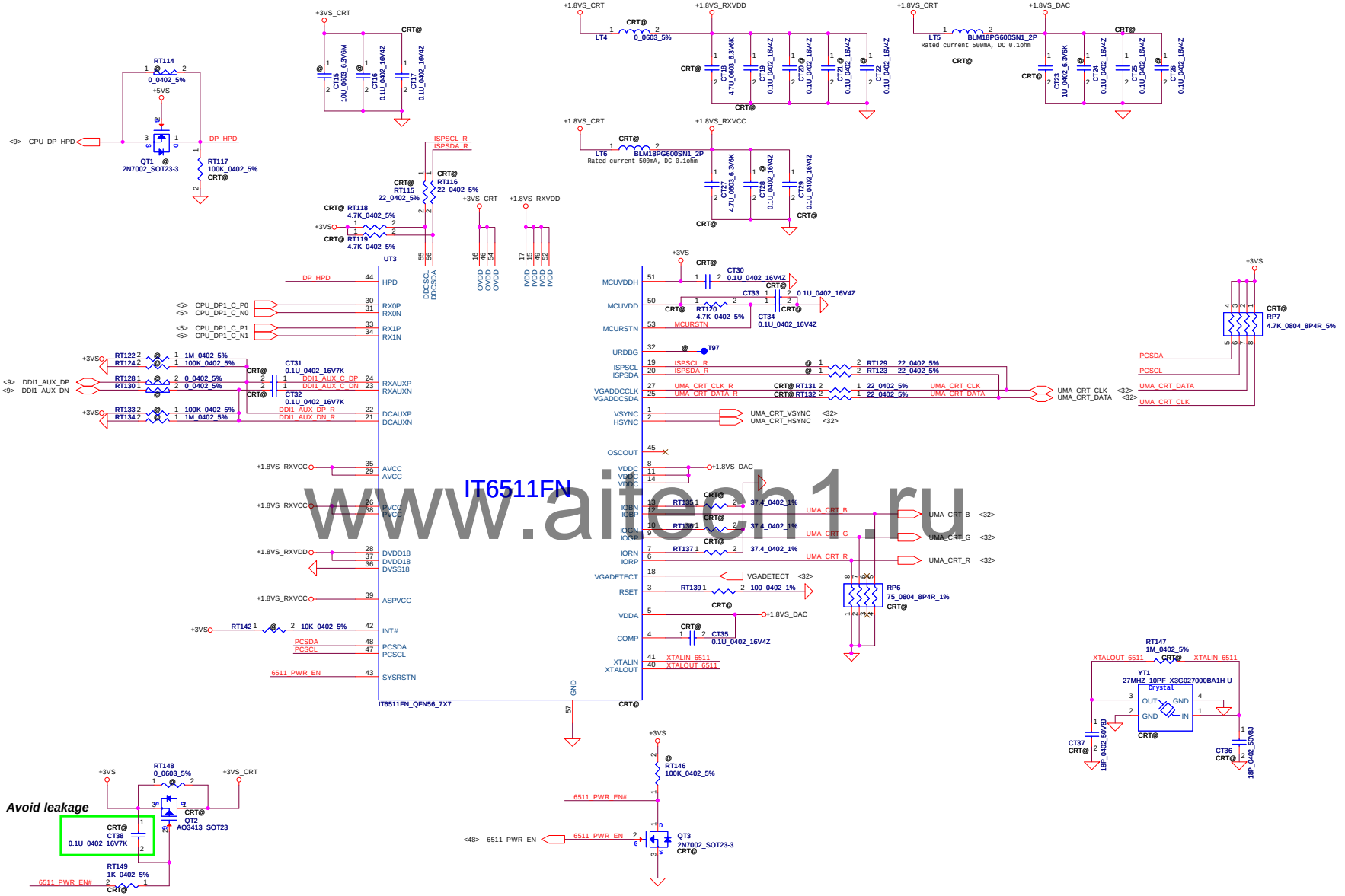


HDMI Connector



Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.			
Title	HDMI Conn.		
Size	Document Number	VSKTA	Rev 1.0
Date: Tuesday, March 19, 2013	Sheet 30 of 53		

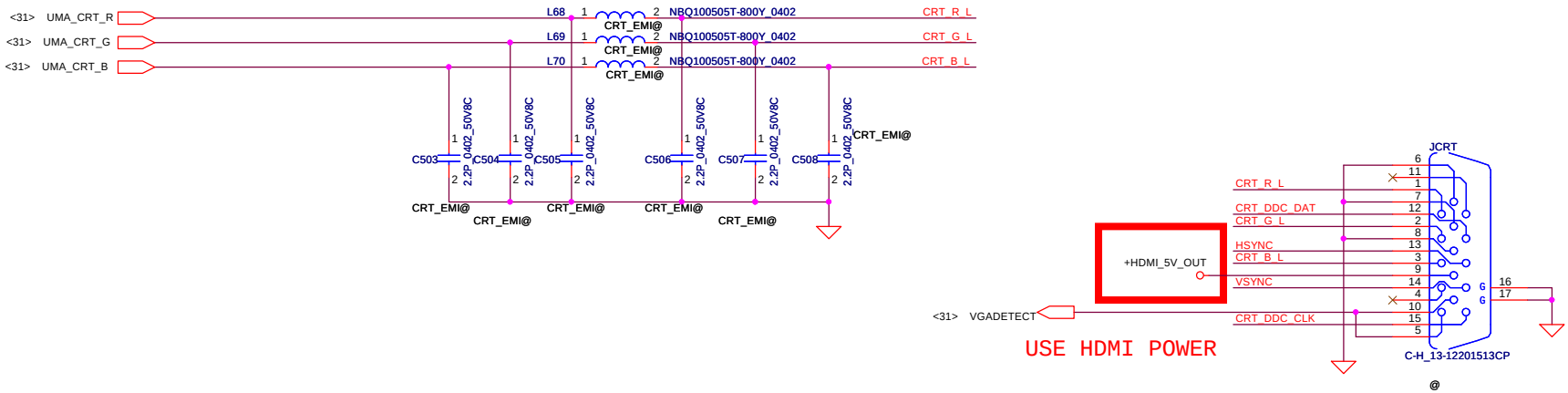


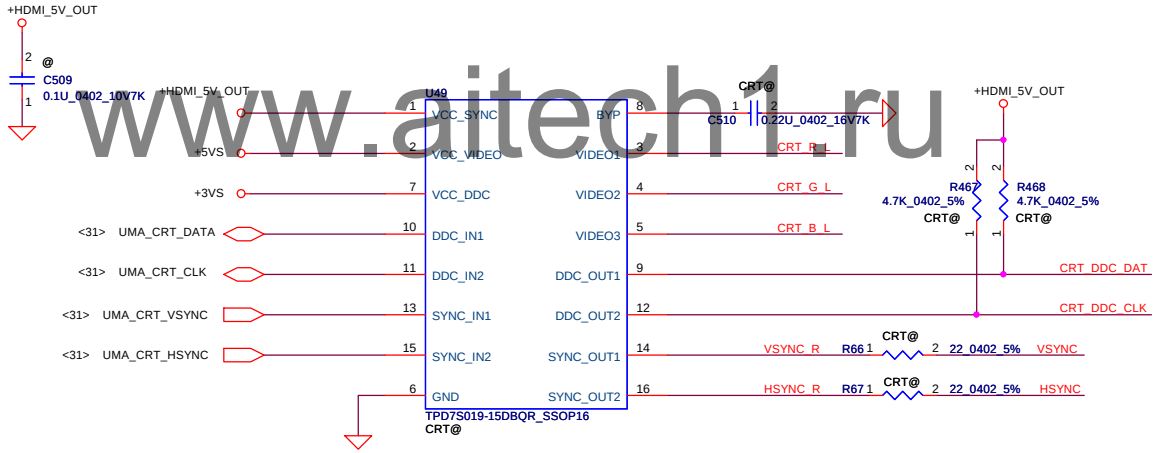
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/09/17	Deciphered Date	Title: DP-CRT_ITE IT6511FN

Size	Document Number		Rev
	DP to VGA		1.0
Date: Tuesday, March 19, 2013		Sheet 31 of 53	

CRT CONNECTOR

BTO : CRT_EMI@



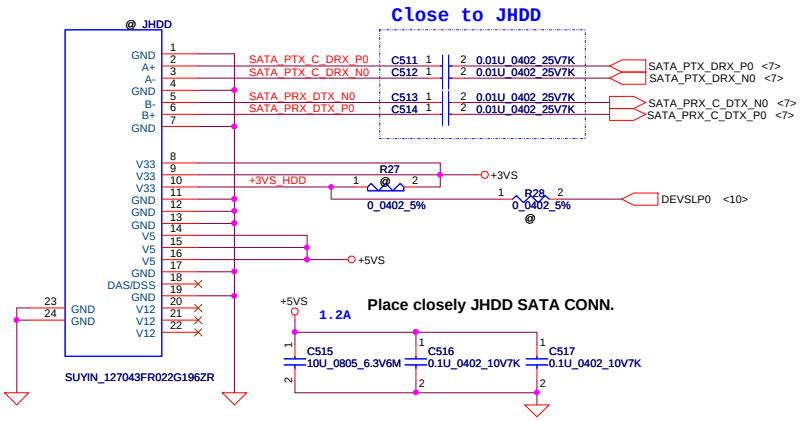


Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

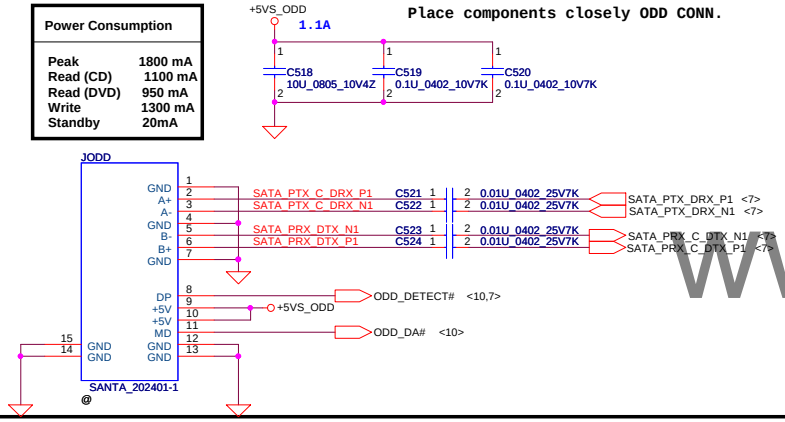
Title	CRT	
Size	Document Number: VSKTA	Rev: 1.0
Date: Tuesday, March 19, 2013	Sheet 32 of 53	

SATA HDD Conn.

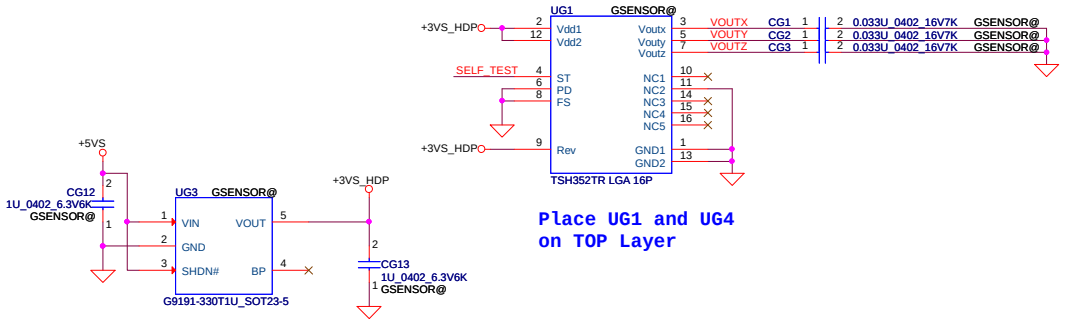


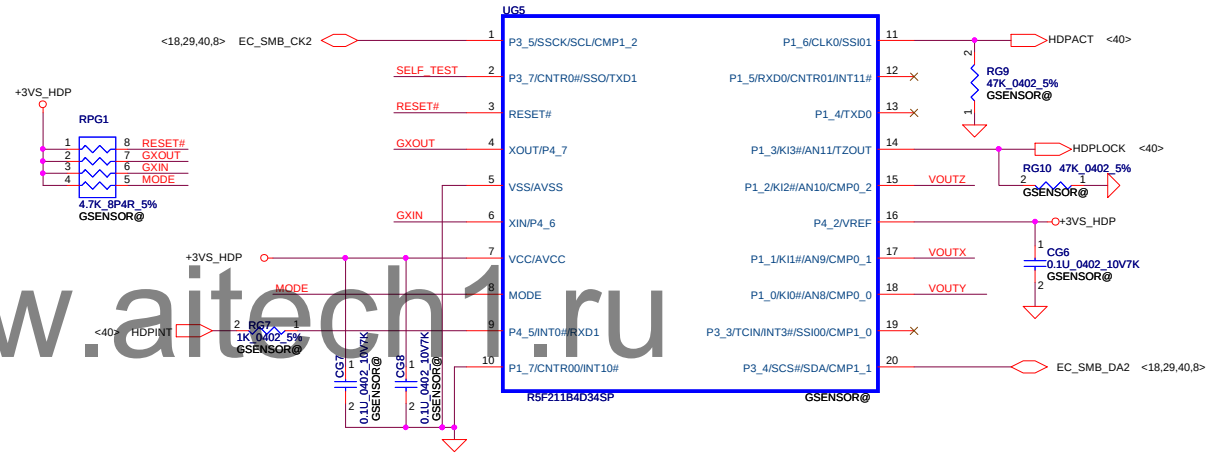
SATA ODD Conn

Power Consumption	
Peak	1800 mA
Read (CD)	1100 mA
Read (DVD)	950 mA
Write	1300 mA
Standby	20mA



G-Sensor





Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.			
Title	HDD/Gsensor		
Size	Document Number	VSKTA	Rev 1.0
Date:	Tuesday, March 19, 2013	Sheet	33 of 53

Slot 1 Half PCIe Mini Card-WLAN

40 mils

+3V_WLAN

0.1U_0402_10V7K

CM1 CM2 CM3

0.1U_0402_10V7K 4.7U_0603_6.3V6K

WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_ON	H	L

From EC

<40> BT_ON — BT_ON — RM26 1K_0402_5% — E51_RXD

For isolate BT_CTRL and Compal Debug Card.

JWLAN

ACES_88914-5204

@

WLAN/ WiFi

WiMax/ BT

<40> WLAN_WAKE# — RC284 Rshort@ — WLAN_WAKE#_R — 0_0402_5%

BT_ON — RM25 @0_0402_5% — BT_CTRL_R

<10,8> CLKREQ_WLAN#

<8> CLK_WLAN#

<8> CLK_WLAN

<11> PCIE_PRX_WLANTX_N4

<11> PCIE_PRX_WLANTX_P4

<11> PCIE_PTX_C_WLANRX_N4

<11> PCIE_PTX_C_WLANRX_P4

+3V_WLAN

<40> E51_TXD — E51_TXD

<40> E51_RXD — E51_RXD

Debug card using

WL_OFF# <40>

PLT_RST_BUF# <35,9>

PM_SMBCLK <16,17,29,41,8>

PM_SMBDATA <16,17,29,41,8>

USB20_N4 <11>

USB20_P4 <11>

LED_WIMAX# <41>

RM6 100K_0402_5% +3VS

DIS only

+3VL — CCL1 GCLK@

+3V_LAN — CCL2 @

+1.05VS_VTT — CCL3 GCLK@

+3VS_DGPU — CCL4 DGCLK@

+3VALW — CCL5 GCLK@

0.1U_0402_10V7K

UCL1 GCLK@

SLG3NB282VTR_TQFN18_2X3P5

+3VL — V3.3A

+3VALW — VDD

+3V_LAN — RCL5 @ 0_0402_5% — +3V_LAN_R — VIO_25M

+1.05VS_VTT — VIOE_24M

+3VS_DGPU — VIOE_27M

DIS only

CLK_X2 — X2

CLK_X1 — X1

GND GND GND

THERMAL_PAD

VBAT

32.768k_A 32.768k_B

24M 25M

27M

VOUT

CCL6 22U_0805_6.3V6M GCLK@

+RTCGCLK — RCL4 120_0603_5% GCLK@ — +RTC

PCH_RTCX1_R <7>

PCH_X1_R_R — LAN_X1_R_R

DGCLK@

VGA_X1_R — RCL3 22_0402_5% — VGA_X1 <18>

DIS only

For safety request

22 ohm for NV chip

GCLK@ 2.2U_0402_6.3V6M CCL9

LAN_X1_R_R — RCL2 @ 0_0402_5% — LAN_X1_R <35>

PCH_X1_R_R — RCL1 @ 0_0402_5% — PCH_X1_R <8>

GCLK@

YCL1 25MHZ 12PF X3G025000DK1H-X

CLK_X1 — CLK_X2

GND GND

CCL7 18P_0402_50V8J GCLK@

CCL8 18P_0402_50V8J GCLK@

Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

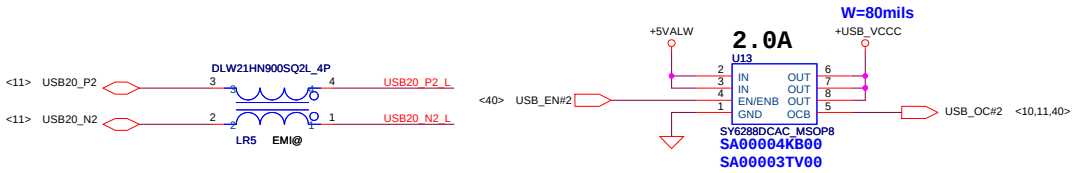
Compal Electronics, Inc.

Title: PCIe-WLAN/mSATA/GCLK

Size | Document Number: VSKTA | Rev: 1.0

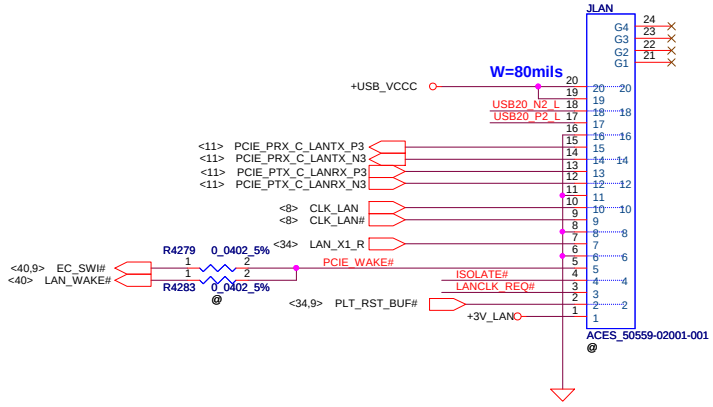
Date: Tuesday, March 19, 2013 | Sheet 34 of 53

Left USB 2.0 x 1



For LAN function

	Sx Enable Wake up	Sx Disable Wake up
WOL_EN#	LOW	HIGH



+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

LAN	WOL	LAN_EN S0	LAN_EN Sx	ISOLATEB S0	ISOLATEB Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

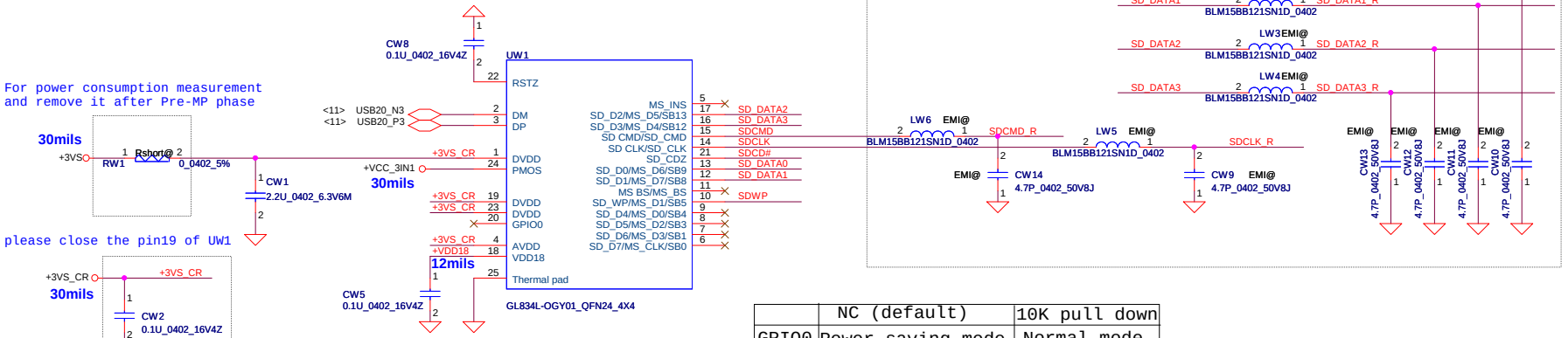
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.

Title: PCIe-LAN-RTL8105E

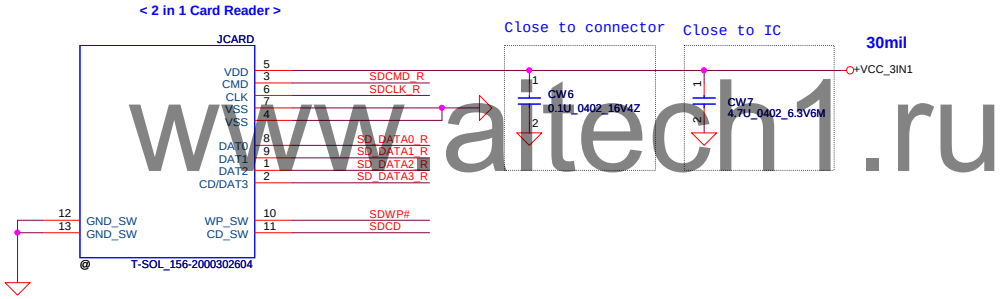
Size: Custom | Document Number: VSKTA | Rev: 1.0

Date: Tuesday, March 19, 2013 | Sheet 35 of 53



	NC (default)	10K pull down
GPIO0	Power saving mode	Normal mode

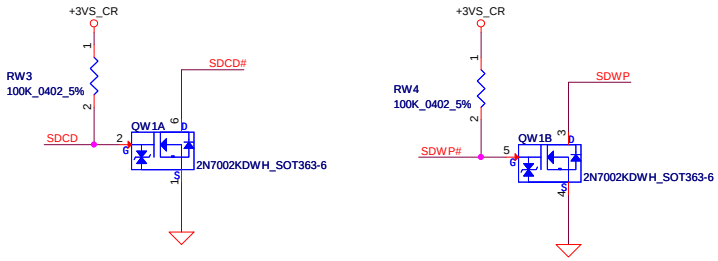
De-coupling and Bulk capacitor should place near to Cardreader chip and Combo Socket



"Normal Close" type connector

	CD_SW	WP_SW	
		Protect disable	Protect Enable
Card Uninsertion	Close	Close	Close
Card Insertion	Open	Open	Close

For normal close type connector invert circuit

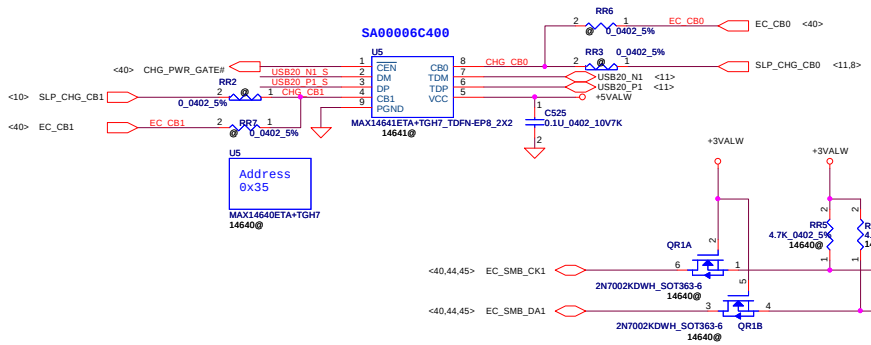


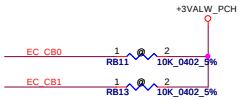
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.			
Title	USB-CardReader Genesys GL834L		
Size: Custom	Document Number: VSKTA		Rev: 1.0
Date: Tuesday, March 19, 2013	Sheet 36 of 53		

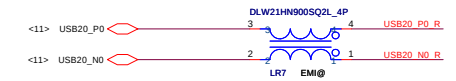
USB Sleep & Charge

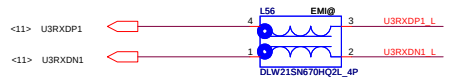
State table for MAX14641			
CB0	**CB1**	**Mode**	**STATUS**
0	0	AM2	2A auto-detection charger mode for Apple device. Resistor dividers are connected to DP/DM. Including DCP
0	1	AP1	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	0	PM	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	CM	USB pass-through mode with CDP emulation. Auto connects DP/DM to TDP/TDM depending on CDP detection status.

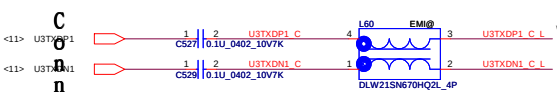


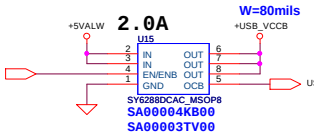


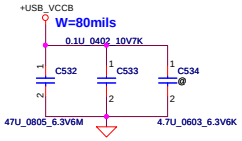
Right rear USB3.0 Conn.

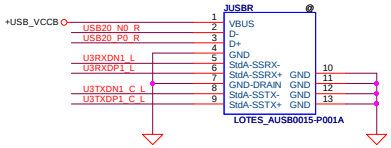


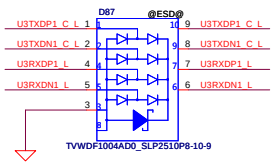




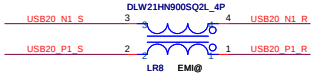


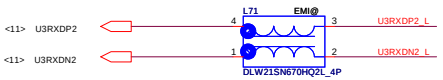


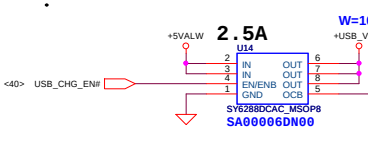


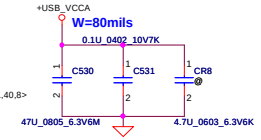


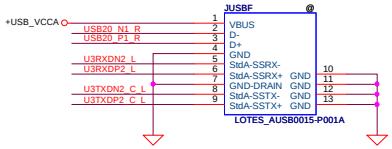
Right Rear USB3.0 Conn.

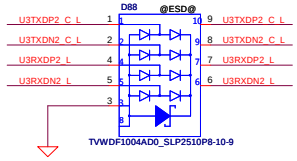




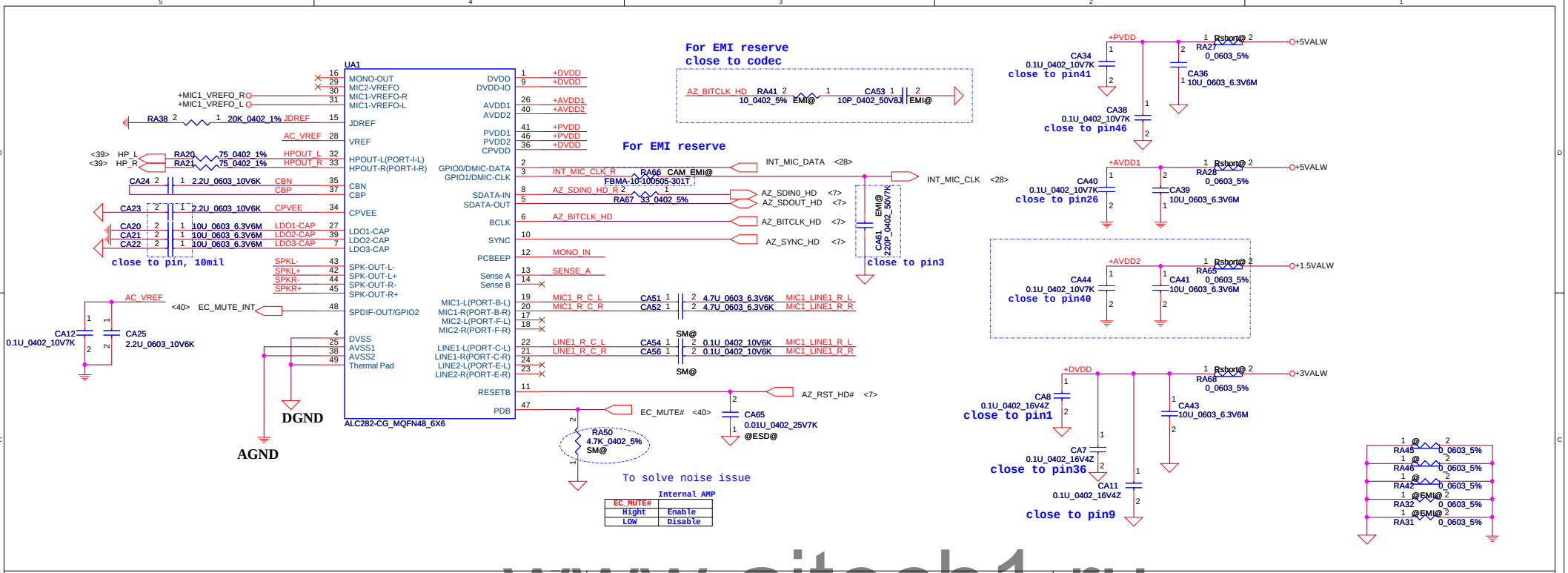




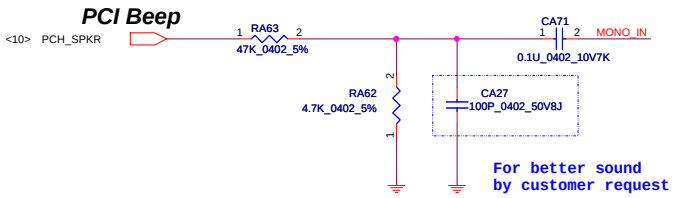




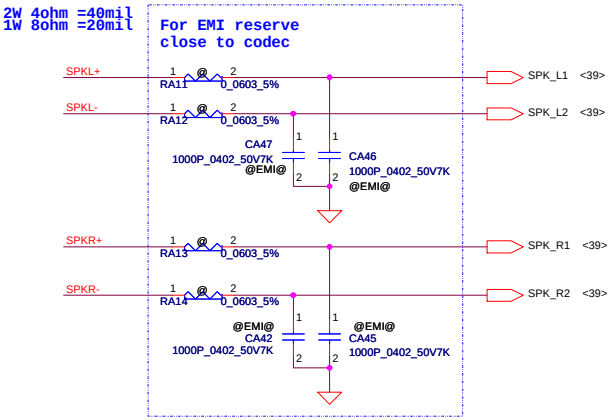
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title RUSB/S&C
Size Custom	Document Number VSKTA		Rev 1.0
Date: Tuesday, March 19, 2013	Sheet 37 of 53		



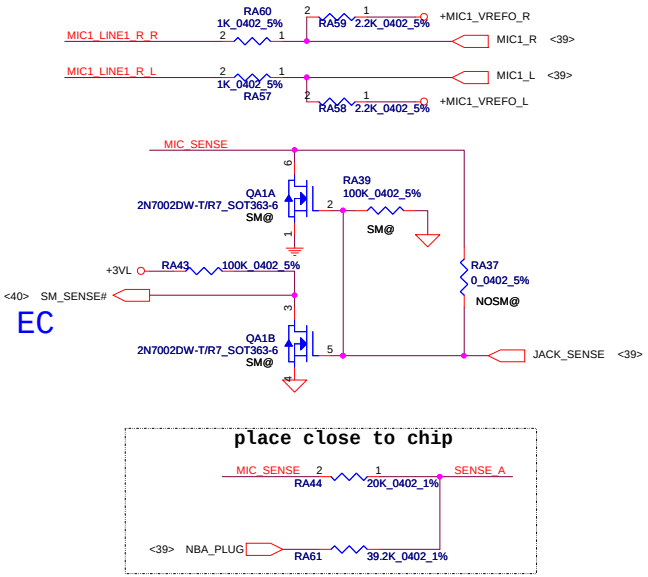
Beep sound



SPK



MIC/LINE IN



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

Security Classification	Compal Secret Data		
Issued Date	2012/07/25	Deciphered Date	2013/07/25

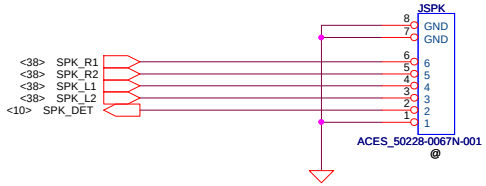
Compal Electronics, Inc.

Title: Cover Sheet

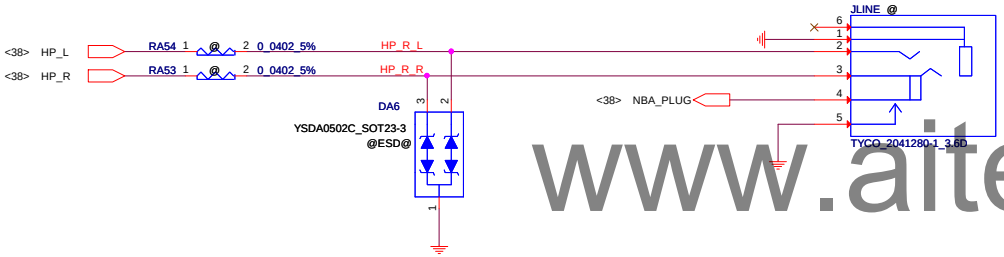
Size: Custom | Document Number | Rev: 1.0

Date: Tuesday, March 19, 2013 | Sheet 38 of 53

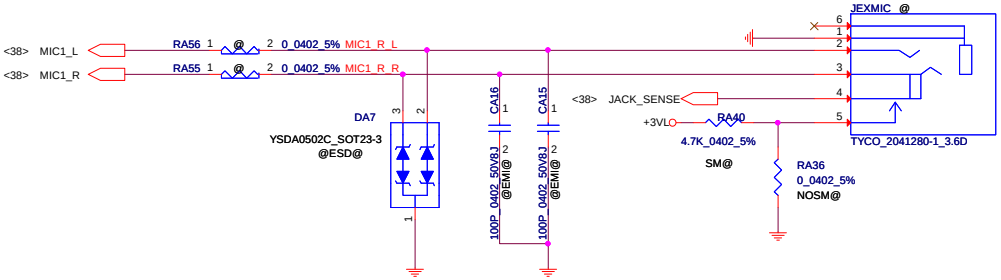
SPK Conn.



HeadPhone/LINE Out JACK

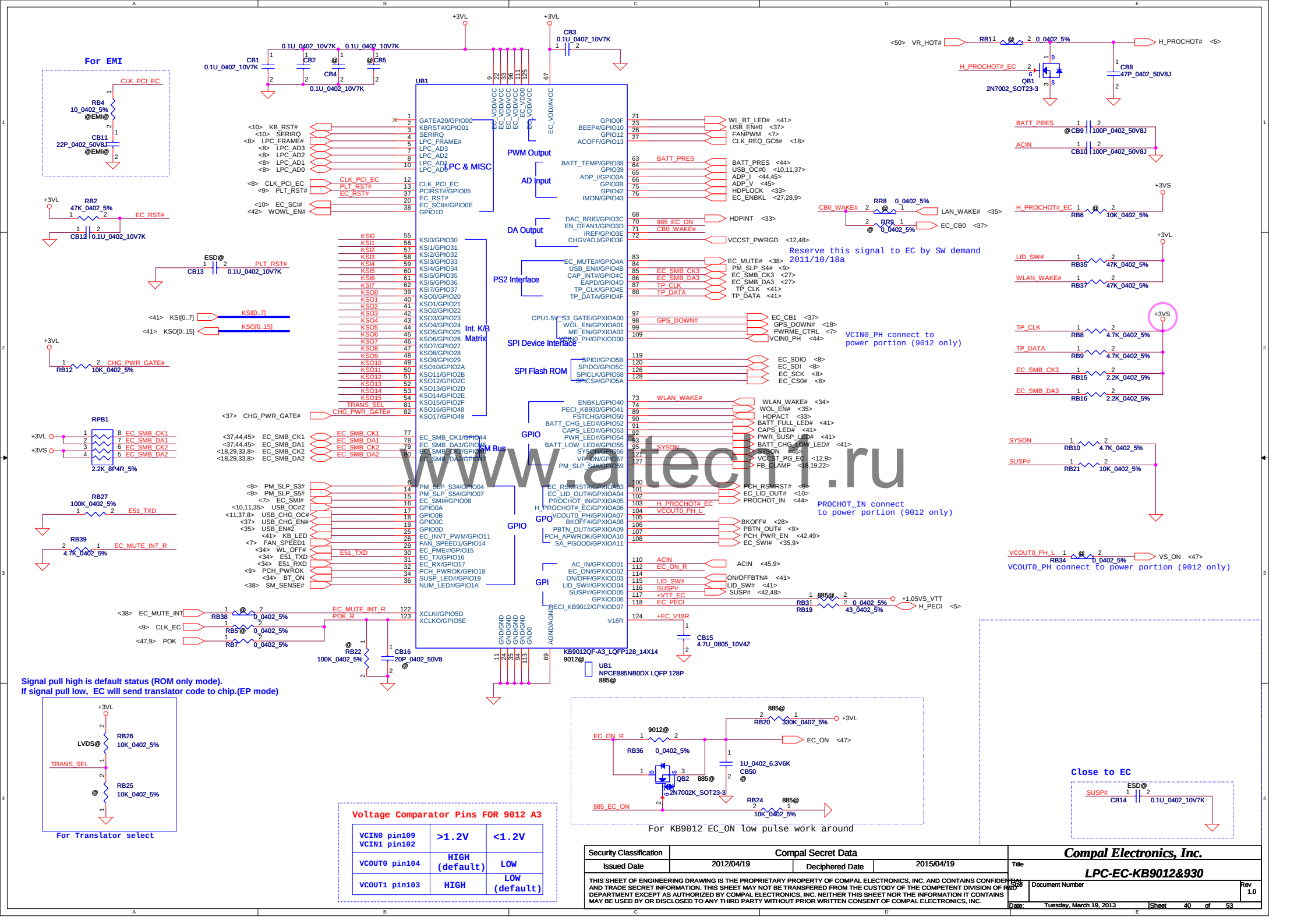


MIC/LINE IN JACK

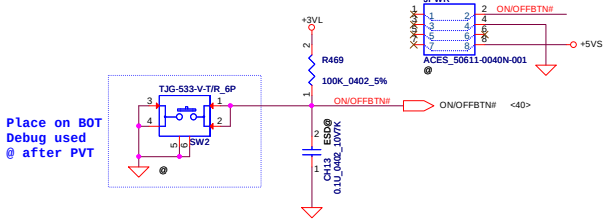


Security Classification	Compal Secret Data		
Issued Date	2012/07/25	Deciphered Date	2013/07/25

Compal Electronics, Inc.			
Title: Conn			
Size: Custom	Document Number		Rev: 1.0
Date: Tuesday, March 19, 2013	Sheet 39 of 53		

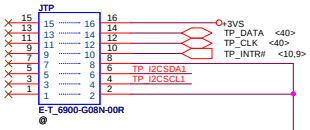


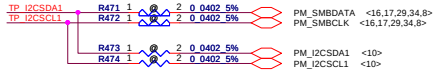
Power Button



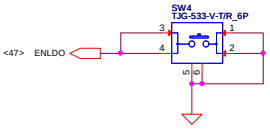
Conn.

Touchpad Connector



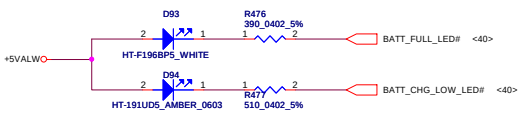


Battery Reset



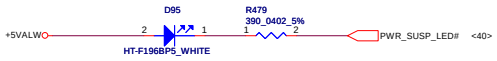
LED/LID

BATT CHARGE /FULL LED



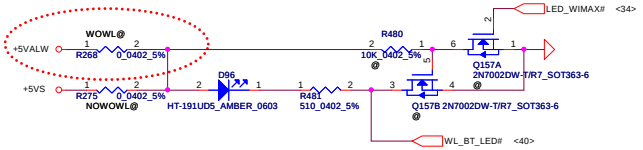
White LED bright when both AC-adaptor is plugged in and Battery is full charged
Amber LED bright while charging battery from AC-adaptor.
Amber LED blink during Critical Low Battery

POWER LED



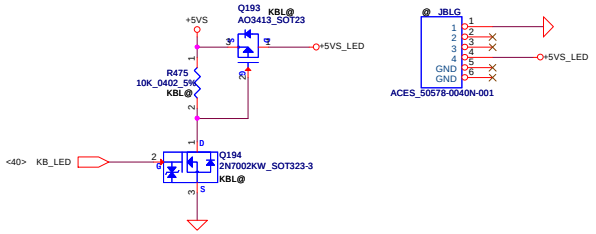
White LED bright when system is power on.
White LED blink when system is sleep mode.

WLAN/WiMAX LED

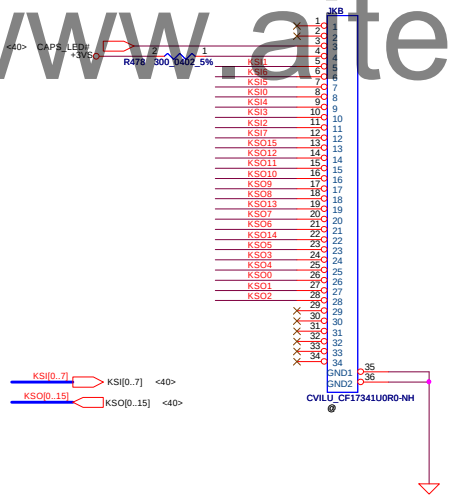


Amber LED bright while Wireless and/or WiMAX turns on.

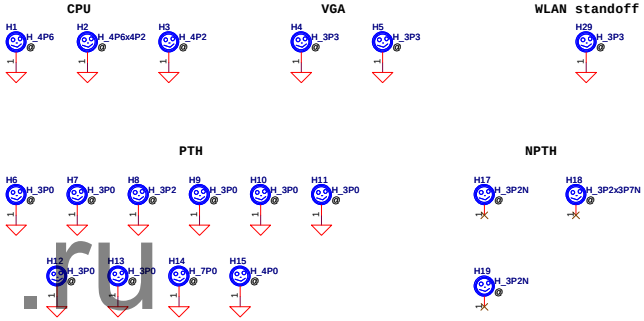
Keyboard LED



NEW KEYBOARD CONN.



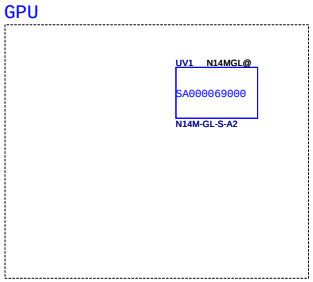
Screw Hole



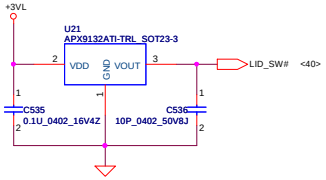
PCB Fedical Mark PAD

ISPD

GPU



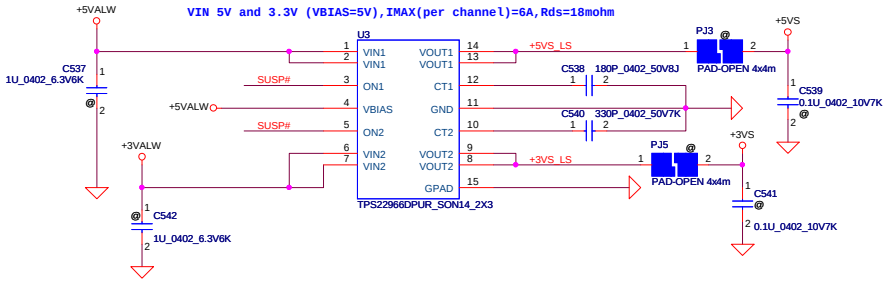
Lid SW



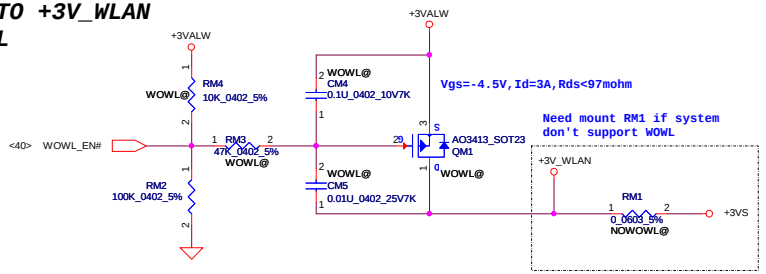
Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.			
Title	TP/ISPD/KB/Screw		
Size	Document Number		Rev
	VSKTA		1.0
Date:	Tuesday, March 19, 2013	Sheet	41 of 53

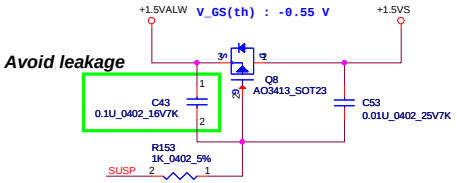
+3VALW TO +3VS
+5VALW TO +5VS
Load Switch

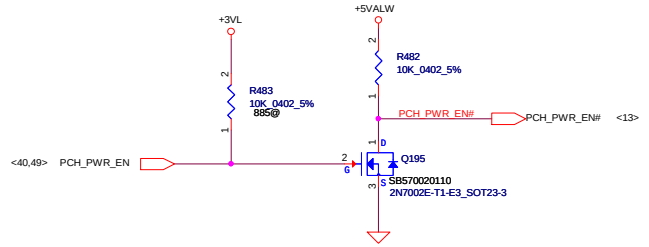


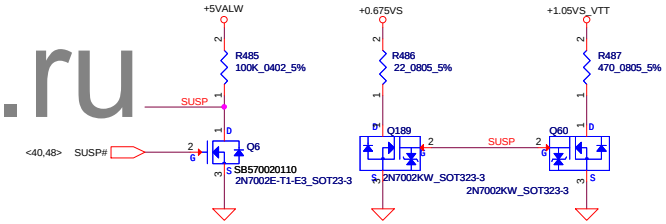
+3VALW TO +3V_WLAN
for WOWL

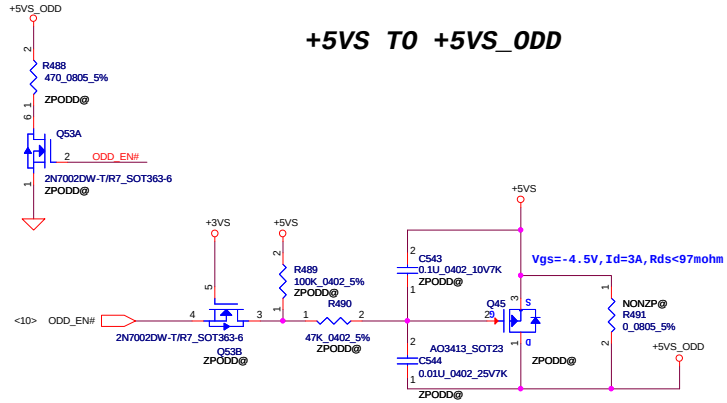


+1.5VALW to +1.5VS





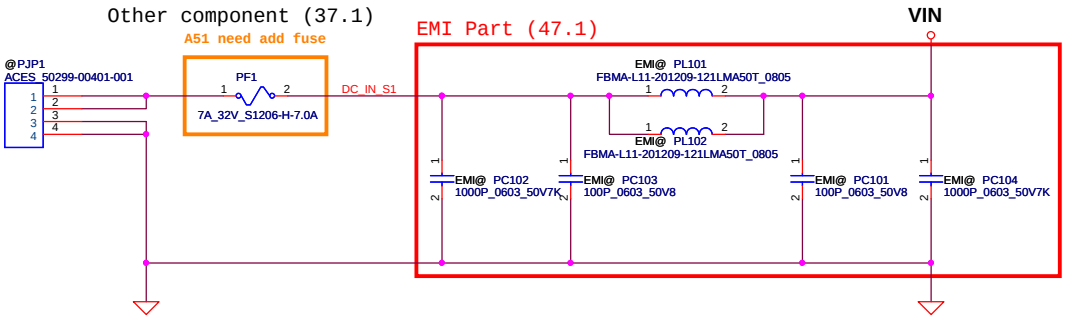


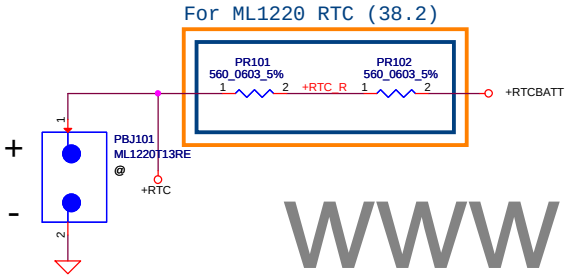


+5VS TO +5VS_ODD

Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

Compal Electronics, Inc.			
Title: DC-DC INTERFACE			
Size	Document Number: VSKTA		Rev: 1.0
Date: Tuesday, March 19, 2013		Sheet 42 of 53	

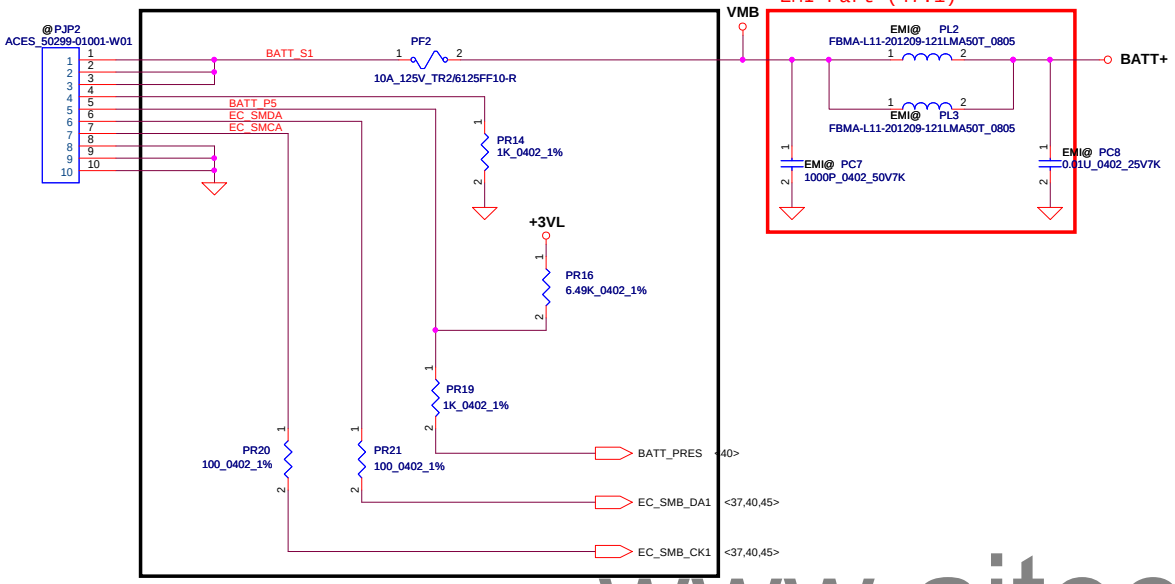




Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	

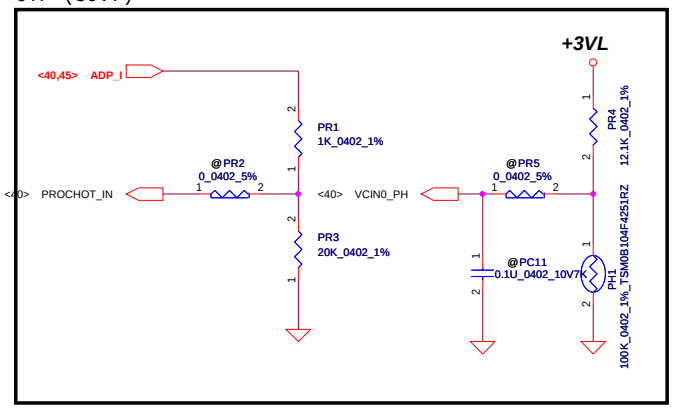
Title	DCIN	
Size	Document Number VSKTA	Rev 0.1
Date:	Sheet 43 of 53	

Other component (37.1)



EMI Part (47.1)

OTP (39.7)

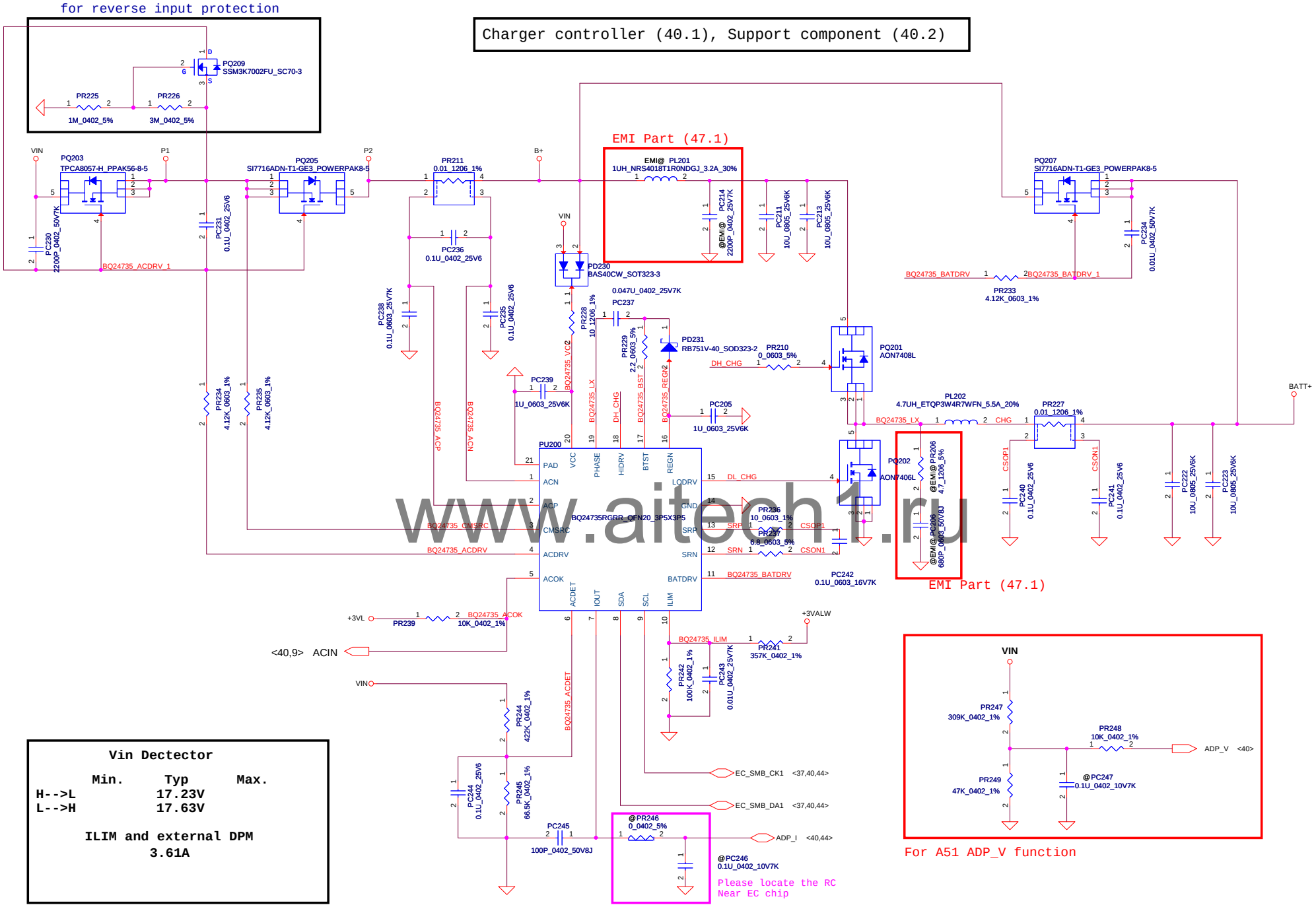


	Initial	Recovery
45W Int GPU	0.55V	0.43V
75W N14P-GV2	0.90V	0.72V

	Initial	Recovery
CPU OTP	90 C	70 C

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: BATTERY CONN / OTP
			Size: Document Number: VSKTA Rev: 0.2
			Date: Sheet 44 of 53

Charger controller (40.1), Support component (40.2)



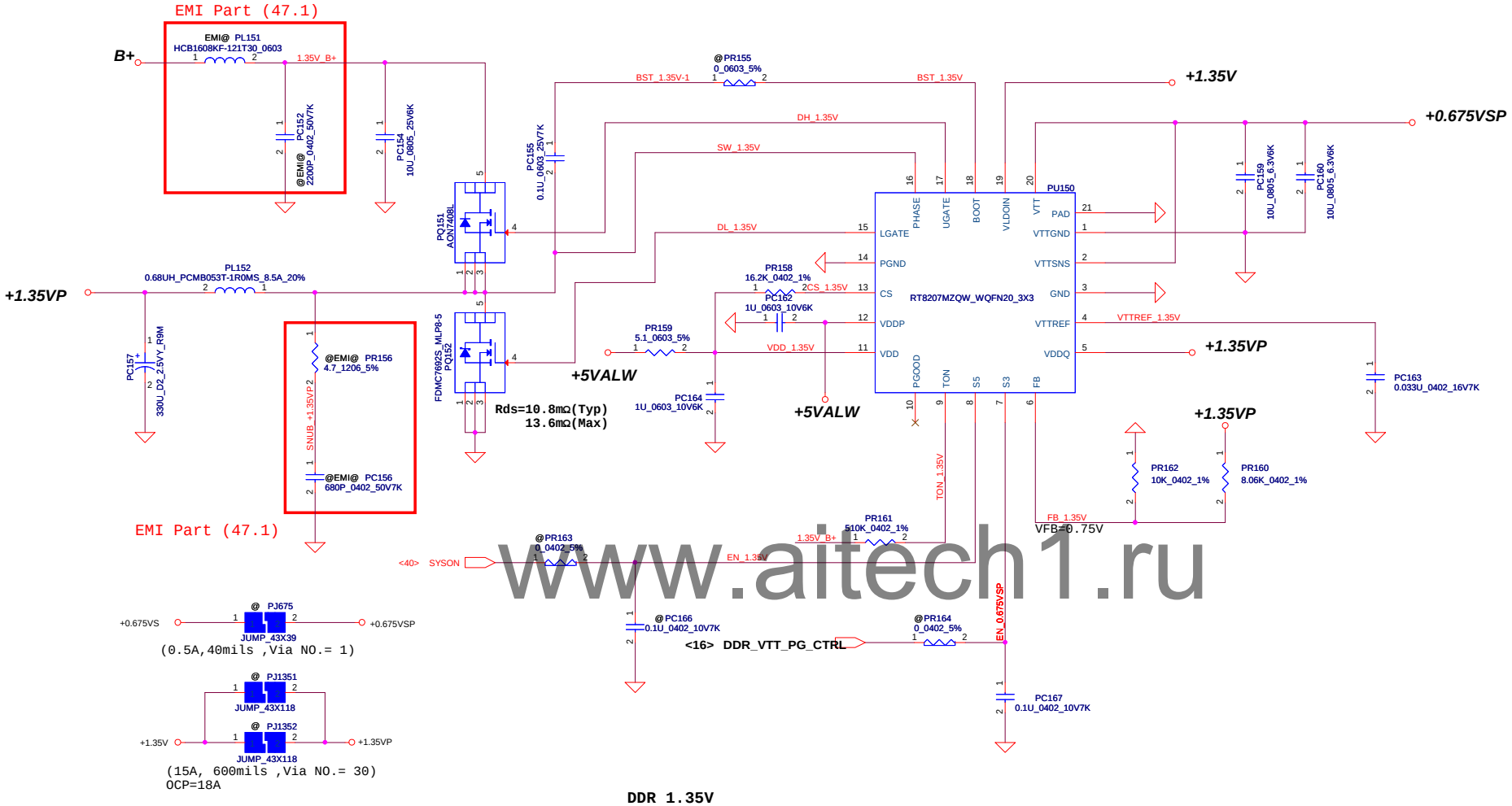
Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L-->H		17.63V	

ILIM and external DPM
3.61A

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: CHARGER
			Size: Document Number: VSKTA Rev: 0.2
			Date: Sheet 45 of 53

DDR controller (35.3), Support component (35.4)



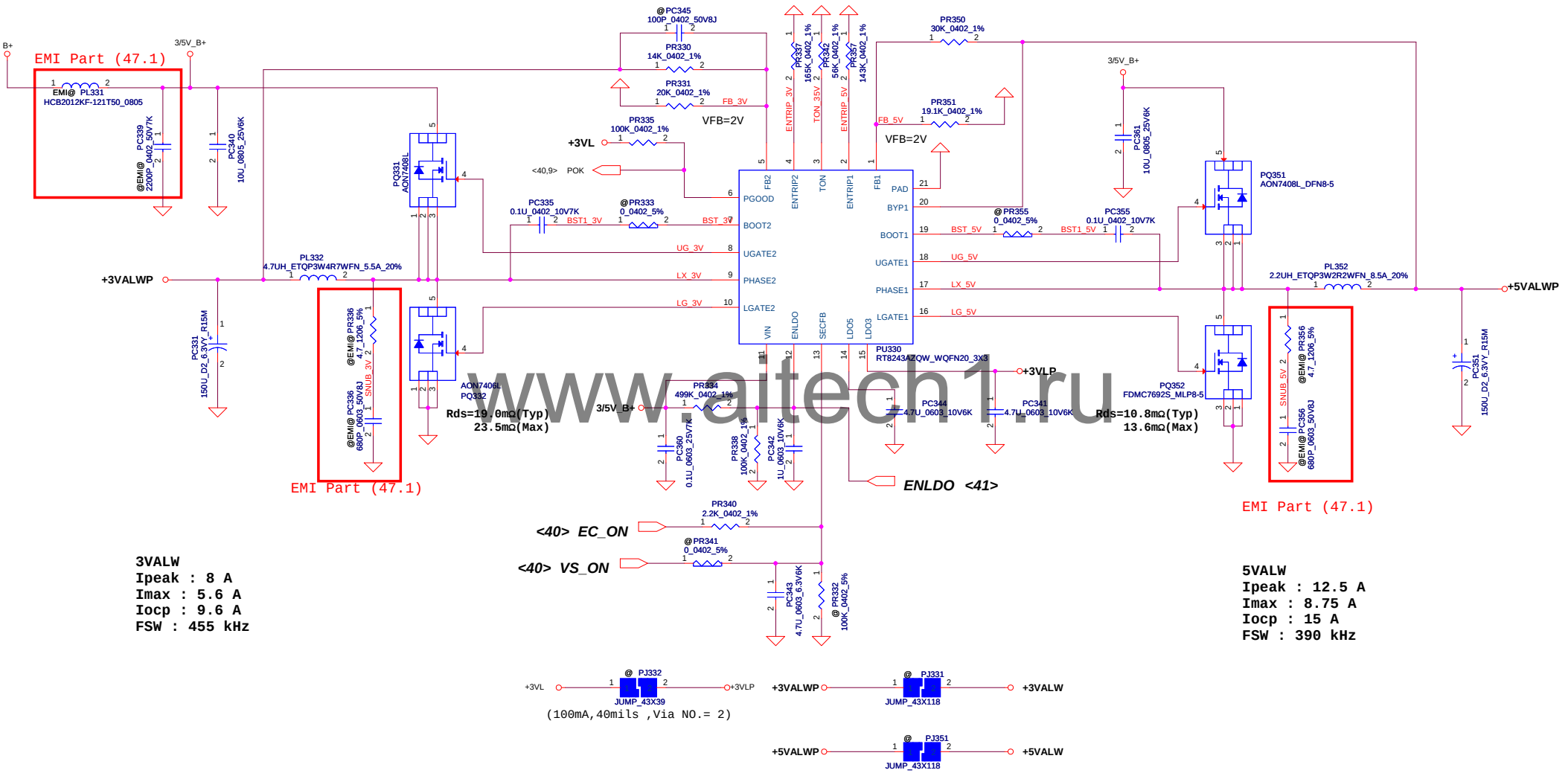
DDR 1.35V
Ipeak : 10 A
Imax : 7A
Iocp : 12 A
FSW : 495 kHz

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

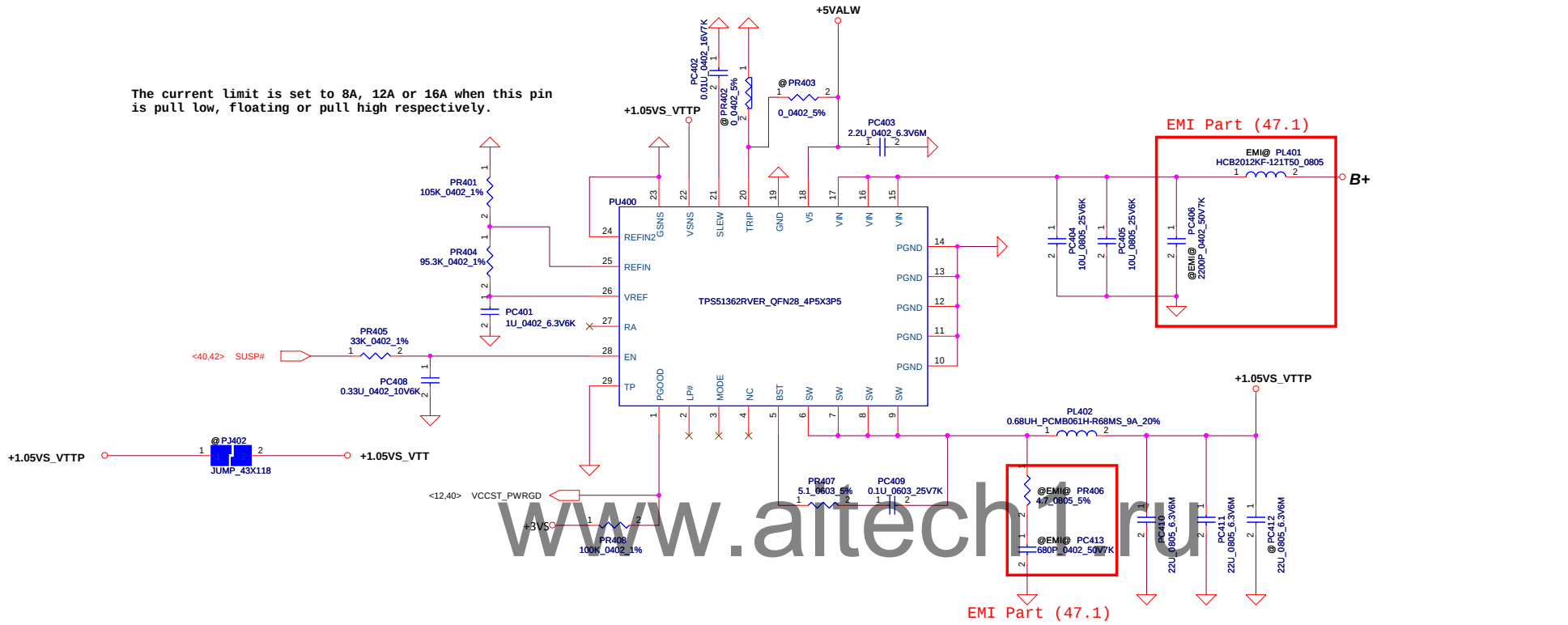
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: 1.35VP/0.675VSP
Size: Custom	Document Number: VSKTA		Rev: 0.2
Date:		Sheet 46 of 53	

3/5VALW controller (35.1), Support component (35.2)

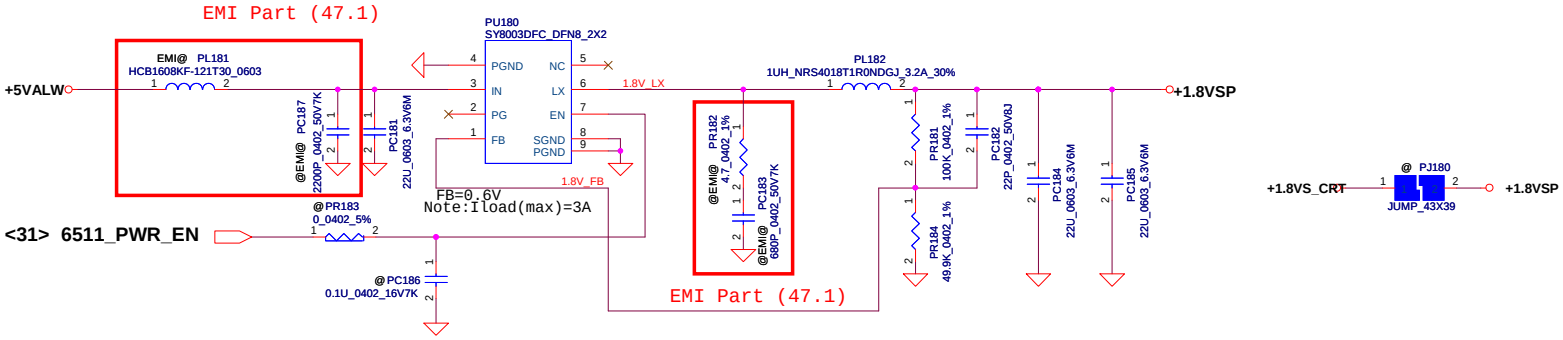


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: 3VALW/5VALW
			Size: Document Number: VSKTA Rev: 0.1
			Date: Sheet 47 of 53

1.05VCCP controller (35.5), Support component (35.6)

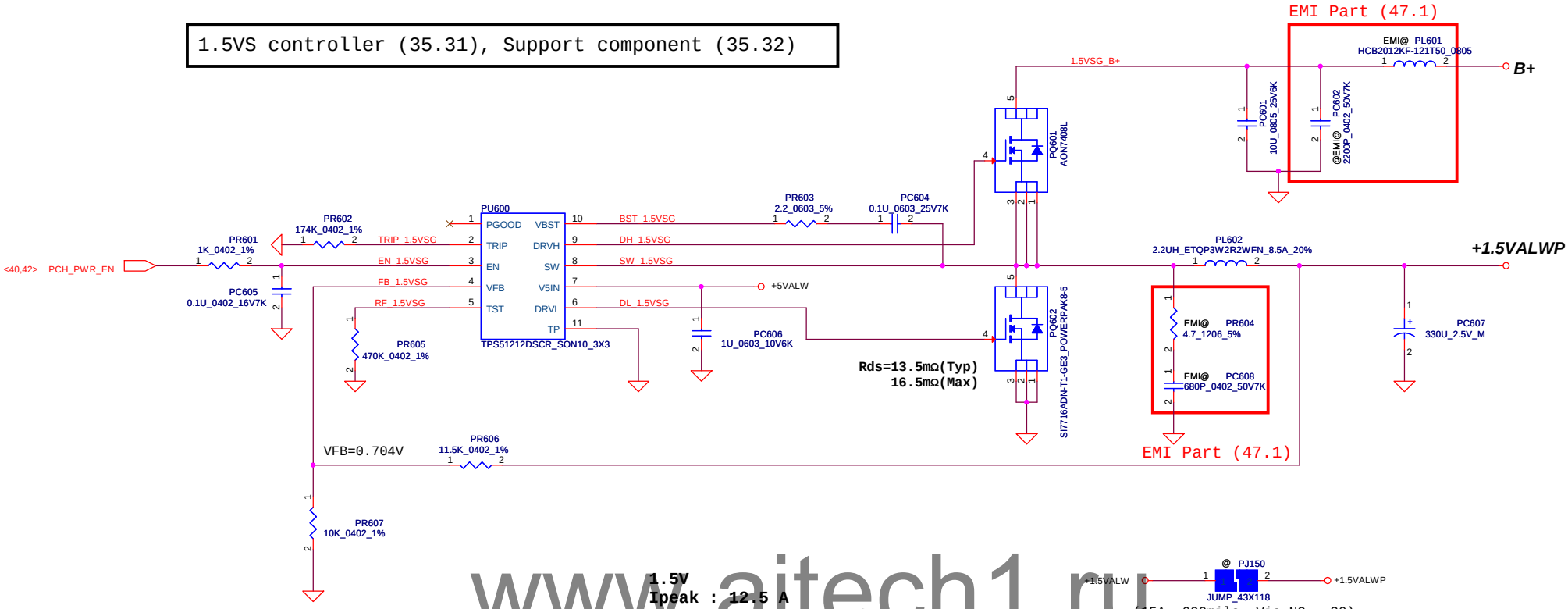


1.8VS controller (35.15), Support component (35.16)



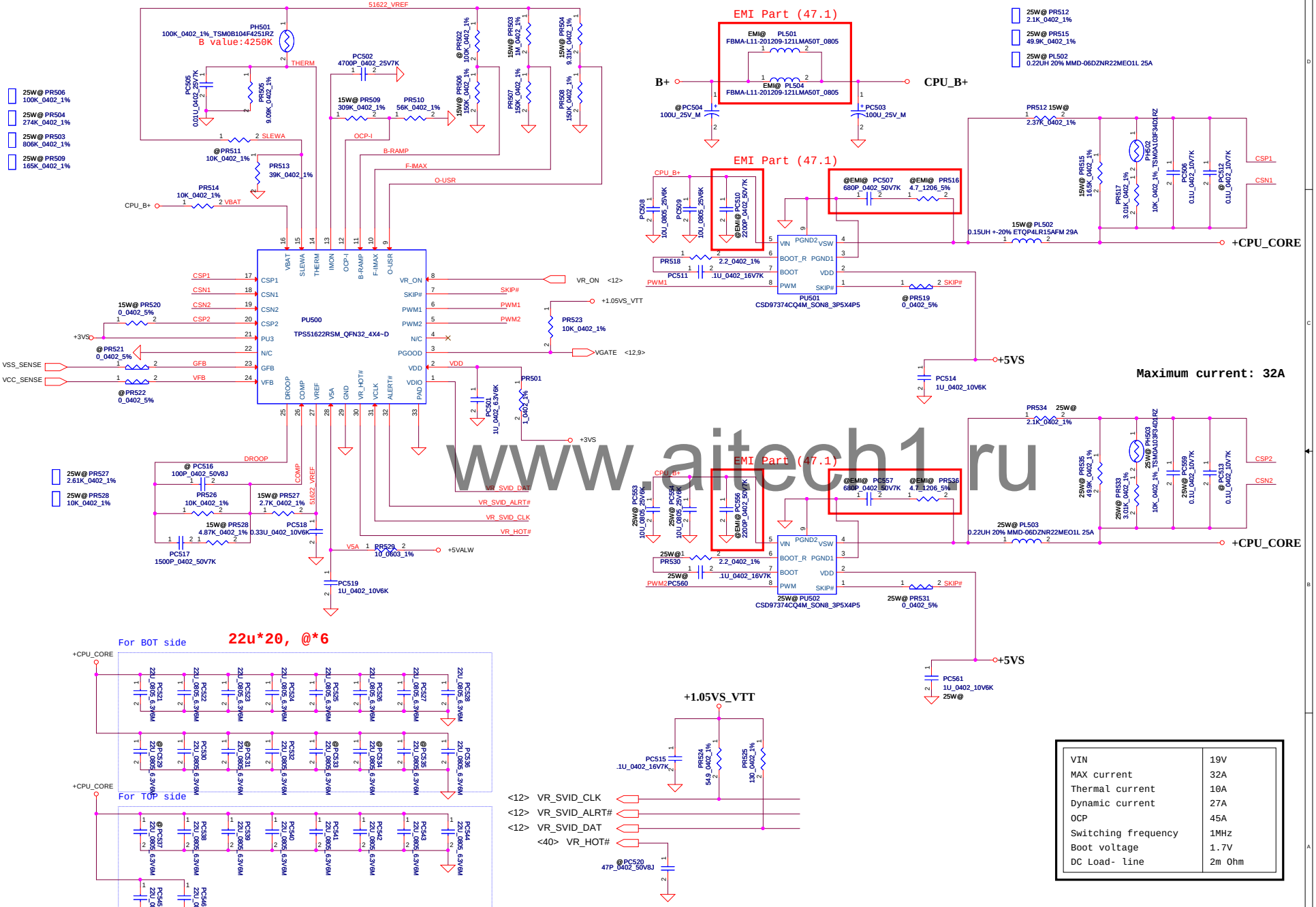
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: +1.05VS_VCCP/1.8VSP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: Document Number: VSKTA; Rev: 0.2; Date: ; Sheet 48 of 53

1.5VS controller (35.31), Support component (35.32)



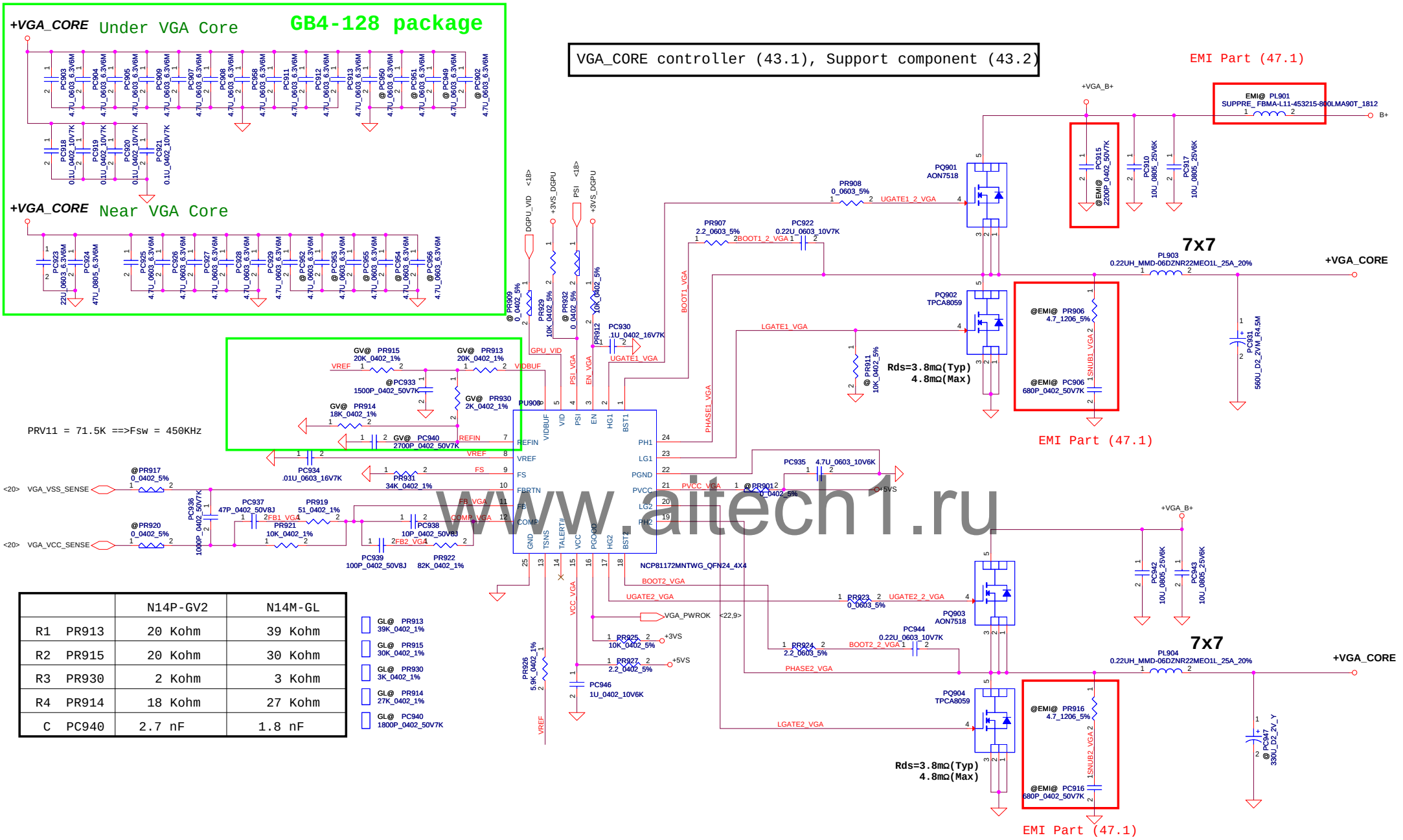
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: +1.5VS
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: Document Number: VSKTA; Rev: 0.2
			Date: Sheet 49 of 53

+VCC_CORE controller (36.1), Support component (36.3)
driver(36.2), decoupling cap(36.4)



VIN	19V
MAX current	32A
Thermal current	10A
Dynamic current	27A
OCP	45A
Switching frequency	1MHz
Boot voltage	1.7V
DC Load- line	2m Ohm

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: CPU_CORE
			Size: Document Number: VSKTA Rev: 0.2
			Date: Sheet 50 of 53



	N14P-GV2	N14M-GL
R1 PR913	20 Kohm	39 Kohm
R2 PR915	20 Kohm	30 Kohm
R3 PR930	2 Kohm	3 Kohm
R4 PR914	18 Kohm	27 Kohm
C PC940	2.7 nF	1.8 nF

GL@ PR913 39K_0402_1%
GL@ PR915 30K_0402_1%
GL@ PR930 3K_0402_1%
GL@ PR914 27K_0402_1%
GL@ PC940 1800P_0402_50V7K

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: VGA_CORE
			Size: Document Number: VSKTA Rev: 0.2
			Date: Sheet 51 of 53

PWR PIR (Product Improve Record)

VSKTA LA-9865P Schematic Change List

Item	Time (When)	Page (Where)	Location / Discription (How / What)	Request (Who)	Reson (Why)
1	EVT--2012/11/28		Add / PC101,PC103,PC102,PC104,PC7,PC8, PL151,PC181,PL2,PC3,PL101,PL102,PL331, PL401,PL601,PL501,PL901	EMI	EMI request
2	EVT--2012/11/28	P50-PWR-CPU_CORE	Value change / PR529,PR520,PR528,PR503, PR507,PR515,PR527,PR509,PR510,PR504,PC516, PL502,PC543,PC544,PC545,PC546,PC514,PC519	PWR	TPS51622 for 15W CPU setting
3	EVT--2012/11/28	P48-PWR-1.05VS_VCCP/1.8VSP	Value change / PR407,PR401,PR404,PR405, PC404,PC405	PWR	For TPS51362 design change
4	EVT--2012/11/28	P46-PWR-1.35VP/0.675VSP	Short pad reserve / PR163	PWR	
5	EVT--2012/11/28	P47-PWR-3VALW/5VALW	PC351 reserve / PC352 mount	PWR	ME limitation
6	EVT--2012/11/28	P50-PWR-CPU_CORE	PC504 reserve	PWR	ME limitation
7	EVT--2012/11/28	P44-PWR-BATTERY CONN / OTP	PF2 change vendor	PWR	for cost down plan
8	EVT--2012/11/29	P46-PWR-1.35VP/0.675VSP	change material / PL152	PWR	For design change
9	DVT-2012/12/13	P43-PWR-DCIN	modify PBJ101 footprint	PWR	for comm footprint
10	DVT-2012/12/13	P44-PWR-BATTERY CONN / OTP	modify PR20,PR21 pin define	PWR	for layout module request
11	DVT-2012/12/13	P46-PWR-1.35VP/0.675VSP	change PR160 to 8.06K	PWR	for output voltage level
12	DVT-2012/12/13	P46-PWR-1.35VP/0.675VSP	modify PL152,PC155,PR164 pin define	PWR	for layout module request
13	DVT-2012/12/13	P47-PWR-3VALW/5VALW	del PC331,PC351	PWR	ME limitation
14	DVT-2012/12/13	P47-PWR-3VALW/5VALW	modify PL332,PR337,PR342,PR357 pin define	PWR	for layout module request
15	DVT-2012/12/13	P47-PWR-3VALW/5VALW	modify the VS_ON direction	PWR	input signal
16	DVT-2012/12/13	P48-PWR-1.05VS_VCCP/1.8VSP	change the 1.8VSP EN to 6511_PWR_EN	PWR	for High enable
17	DVT-2012/12/13	P48-PWR-1.05VS_VCCP/1.8VSP	modify PR401,PC402,PR182 pin define	PWR	for layout module request
18	DVT-2012/12/13	P49-PWR-1.5VALWP	change PR603 to 0ohm	PWR	VBST resistor
19	DVT-2012/12/13	P49-PWR-1.5VALWP	modify PR602,PR606,PL601 pin define	PWR	for layout module request
20	DVT-2012/12/13	P50-PWR-CPU_CORE	change the B+ EMI bead	PWR	ME limitation
21	DVT-2012/12/13	P50-PWR-CPU_CORE	modify PC516,PR526,PR527,PC517,PR529,PR512, PR516,PR518,PR534,PR536,PR530,PR524 pin define	PWR	for layout module request
22	DVT-2012/12/13	P51-PWR-VGA_CORE	PR912/add 10K ohm	PWR	pull high +3VS_DGPU
23	DVT-2012/12/13	P51-PWR-VGA_CORE	PC934 change to 0.01u	PWR	VREF pull down cap
24	DVT-2012/12/13	P51-PWR-VGA_CORE	modify PL901,PR908,PR907,PR901,PR923,PR924, PR927,PC946,PR913,PR915,PR914,PR904,PR928, PR931,PR932,PR909 pin define	PWR	for layout module request
25	PVT-2013/01/25	P47-PWR-3VALW/5VALW	change PC332,PC352,PR409 location to PC331,PC351,PR335	PWR	common change
26	PVT-2013/01/25	P46-PWR-1.35VP/0.675VSP	change PL152 value from 1uH to 0.68uH	PWR	for design change
27	PVT-2013/01/25	P46-PWR-1.35VP/0.675VSP	change PC157 to 390uF 5*5.7	PWR	layout request
28	PVT-2013/01/25	P51-PWR-VGA_CORE	change PC934 part number	PWR	common change
29	PVT-2013/02/04	P50-PWR-CPU_CORE	PC529,531,533,534,535,537 reserve PC505 0.1uF change to 10nF PR527 4.99k change to 2.7k PR509 374k change to 309k PC506 0.15u change to 0.1u PR510 39k change to 56k	PWR	for TPS51622 date code 2BI design change
30	PVT-2013/02/04	P51-PWR-VGA_CORE	PC947 330u reserve	PWR	for cost down plan
31	PVT-2013/02/04	P51-PWR-VGA_CORE	PL903,904 change PN	PWR	common change
32	PVT-2013/02/04	P49-PWR-1.5VALWP	net name change from 1.5VALW_EN to PCH_PWR_EN	HW	for common design change
33	PVT-2013/02/07	P49-PWR-1.5VALWP	PR604 PC608 mount PR603 change from 0ohm to 2.2ohm	EMI	EMI request
34	PVT-2013/02/07	P49-PWR-1.5VALWP	PL602 change from 4.7u to 2.2u	PWR	For design change
35	PVT-2013/02/07	P48-PWR-1.05VS_VCCP/1.8VSP	PL402 change PN from RX00 (H1.8) to 5K80 (H3.0)	PWR	change Material for useful height
36	PreMP-2013/03/18	P46-PWR-1.35VP/0.675VSP	PC157 footprint change to C_D2	PWR	
37	PreMP-2013/03/18	P46-PWR-1.35VP/0.675VSP	PR155 0 ohm resistor change to short pad	EMI	EMI request
38	PreMP-2013/03/18	P47-PWR-3VALW/5VALW	PR333,PR355 0 ohm resistor change to short pad	EMI	EMI request
39	PreMP-2013/03/18	P46-PWR-1.35VP/0.675VSP	PR164 0 ohm resistor change to short pad	HW	HW requset

HW PIR (Product Improve Record)

VSKTA LA-9865P Schematic Change List

REVISION: 0.1 to 0.2

Item	Date	Page	Solution	Request
1.	12/05	P37	Update CHG_CB1,0 level shifter (QR1) circuit	For USB S & C level shifter circuit
2.	12/05	P37	U5.1 (CHG_PWR_GATE#) was connected to the EC(GPIO49) Pin82	For USB S & C
3.	12/05	P40	Add pull high RB12 to +3VL on CHG_PWR_GATE#	For USB S & C
4.	12/05	P32	Add R66,R67 22ohm for CRT undershoot issue	For CRT VSYNC and HSYNC
5.	12/05	P18	Rotate DV1	For GC6
6.	12/05	P18	FB_CLAMP_MON be pulled up to +3VS_DGPU on RPV12.6	For GC6
7.	12/05	P22	Change UV2 from SA007320120 to SA007320300	For GC6
8.	12/05	P40	Change PM_SLP_S4# from UB1.127 to UB1.84	For EC GPIO setting
9.	12/05	P40	Change USB_EN#0 from UB1.84 to UB1.23.	For EC GPIO setting
10.	12/05	P40	Change FB_CLAMP from UB1.23 to UB1.127.	For EC GPIO setting
11.	12/06	P18	Change CV9,CV10,CV11,CV12,CV13,LV1 to OPT@	For DIS BOM config.
12.	12/06	P18	Change RV8 from OPT@ to DGCLK@	For DIS GCLK config.
13.	12/06	P18,34	Change 27M_R to VGA_X1	For VGA CLK
14.	12/06	P34	Change 27M to VGA_X1_R	For VGA CLK
15.	12/06	P31	Change RT128, RT130 to 0 ohm short pad.	For DP to CRT circuit
16.	12/06	P31	Change RT129, RT123 from CRT@ to @.	For DP to CRT circuit
17.	12/06	P31	Change RT140,RT141,RT138 to RP6 (75 ohm row resistor).	For DP to CRT circuit
18.	12/06	P31	Change RT121,RT126,RT143,RT144 to RP7 (4.7K ohm row resistor).	For DP to CRT circuit
19.	12/07	P09	Change RH17 from IEDP@ to LVDS@	For LVDS panel backlight control
20.	12/07	P09	Change RH18 from LVDS@ to IEDP@	For LVDS panel backlight control
21.	12/07	P29	Change R23,R24 from @ to mount	For SMBUS control by EC
22.	12/07	P29	Change R25,R26 from mount to @	For SMBUS control by EC
23.	12/07	P30	Change L64,L65,L66,L67 from SM070001S00 to SM070001R00.	For HDMI choke
24.	12/10	P08	Change UH3,UH4 from 45@ to always mount.	For DVT build
25.	12/10	P10	Change R274,R272 from mount to @	For touch pad function
26.	12/10	P29	Change UY3,CY26 from EHDMI@ to 8201@	For touch pad function
27.	12/11	P29	Delete RT125,RT127	For DP to CRT ISP programming data pin
28.	12/12	P38	Change CA51,CA52 from 2.2uF to 4.7uF	Follow Codec ALC269 common design
29.	12/13	P32	Delete R464,R465,R466	For CRT impedance matching resistors
30.	12/13	P30	Mirror vertically for L64,L65,L66,L67	For HDMI choke layout
31.	12/13	P27	Swap RP5 net name	For EDP row resistor layout
32.	12/17	P31	Swap RP6,RP7 net name	For DP to CRT row resistor layout
33.	12/18	P08	Delete UH4,RH96,RH97,RH92,RH93,RH94,CH10	Remove SPI ROM for Win8 (2MByte) circuit
34.	12/18	P08	Change UH3 from SA00003K820 to SA00006MK00	Change SPI ROM to 8MByte
35.	12/18	P08,40	Change EC_CS1# to EC_CS0#	For 8MB SPI ROM
36.	12/18	P08	Delete PCH_SPICS1#	For use 8MB SPI ROM
37.	12/18	P08	Change UH3.1 from PCH_SPICS1# to PCH_SPICS0#	For use 8MB SPI ROM
38.	12/20	P27	CT9 change to 10UF (the same as CT4)	For use 8MB SPI ROM
39.	12/20	P27	Delete LT3 and +SWR_LX then short +SWR_V12 to UT2.12	For LVDS Translator
40.	12/20	P27	Delete EC_SMB_CK3 and EC_SMB_DA3	For LVDS Translator
41.	12/20	P27	UT2 change to RTD2132R	For LVDS Translator
42.	12/20	P27	UT2 change 2132S@ to LVDS@	For LVDS Translator
43.	12/20	P27	Change UT2.15 from TL_ENVDD to +LCD_VDD	For LVDS panel control
44.	12/20	P27,28	Delete TL_ENVDD	For LVDS panel control
45.	12/20	P27	Delete RT106	For LVDS
46.	12/20	P28	Delete R429	For LVDS
47.	12/20	P27	Change RT4,RT7 from 2132S@ to @	For LVDS
48.	12/20	P27	Change RT6,RT12 from 2132R@ to LVDS@	For LVDS
49.	12/20	P28	Change U18,C475,R426,R430 from 2132S@ to IEDP@	For LCD power circuit
50.	12/20	P28	Delete C475,U18,R430,R426 IEDP symbol	For LCD power circuit
51.	12/20	P29	Change UY3 symbol from SA00005CW00 to SA00005CW10	For HDMI re-driver

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: HW-PIR

Size: D26 Custom	Document Number		Rev 1.0
Date: Tuesday, March 19, 2013	Sheet 53 of 53		

HW PIR (Product Improve Record)

VSKTA LA-9865P Schematic Change List
REVISION: 0.2 to 0.3

Item	Date	Page	Solution	Request
1.	01/21	P38,40	Add EC_MUTE_INT	For audio codec
2.	01/21	P31	Update ISPSCL /ISPSDA connection	For CRT
3.	01/30	P18,40	UV1 GPIO12 (GPS_DOWN#) be connected to EC GPXIOA01	For GPS
4.	01/30	P28	Change L61 form TOUCH@EMI@ change to TOUCH_EMI@	For EMI BOM Config
5.	01/30	P32	Change L68,L69,L70,C503,C504,C505,C506,C507,C508 form CRT@EMI@ change to CRT_EMI@	For EMI BOM Config
6.	02/01	P28	Delete R426 and change U18.1 connected to +LCD_VDD	For LVDS
7.	02/01	P28	Delete R427 and change U18.3 connected to LCD_ENVDD	For LVDS
8.	02/01	P40	Change UB1.81 from PCIE_WAKE# to TRANS_SEL, and add pull-high resistor RB26 and reserve RB25 to GND	For LVDS
9.	02/01	P35	PCIE_WAKE# add R4279 and reserve R4283 to LAN_WAKE# to EC	For WAKE function
10.	02/01	P9	Change RH171 from 10Kohm to 1Kohm	For WAKE function
11.	02/01	P9	Delete RH136 and change U1.AJ5 from PCIE_WAKE#_R to WAKE# and connected to R4279.1 and RH171.1	For WAKE function
12.	02/01	P35	Add RC284 between JWLAN.1 to WLAN_WAKE#	For WAKE function
13.	02/01	P28	Add DA8 on INT_MIC_CLK	For ESD's request
14.	02/01	P28	Add DA9 on INT_MIC_DATA	For ESD's request
15.	02/01	P28	Reserve D97 on USB20_P7_R, USB20_N7_R	For ESD's request
16.	02/04	P10	Reserve D98 to GND on H_THERMTRIP#	For ESD's request
17.	02/04	P41	Reserve D99 to GND for ON/OFFBTN#	For ESD's request
18.	02/04	P28	Delete R427 and U18.3 connected to LCD_ENVDD	For LVDS
19.	02/04	P28	Add R4280, R4281 to co-layout L61	For LVDS
20.	02/04	P40	Change RB135,RB136 BOM config from LVDS@ to @	For LVDS
21.	02/08	P29	Change RY33 from 4.99Kohm to 4.3Kohm	For HDMI test
22.	02/08	P42	Change RM4 from 100Kohm to 10Kohm	For WLAN issue
23.	02/08	P38	Change RA41, CA53 from @EMI@ to EMI@	For EMI 216MHz noise (24MHz harmonic).
24.	02/08	P40	Change QB1 from SB000009080 to SB570020020	For EL code
25.	02/21	P28	Change L61 from TOUCH_EMI@ to @TOUCH_EMI@	For EMI touch
25.	02/21	P28	Add R4280,R4281 on USB20_P5/USB20_N5	For EMI touch
26.	02/23	P36	Change RW2 from 0ohm to 33ohm	For EMI's request
27.	02/23	P36	Change CW9 BOM config from @EMI@ to EMI@.	For EMI's request
28.	02/23	P31	Change YT1 from SJ10000DK00 to SJ100009700	For crystal vendor's recommend
29.	02/23	P28,35,37	Change L61,L62,LR5,LR7,LR8 from SM070000K00 to SM070001N00.	For EMI's request
30.	02/23	P30	Change L64,L65,L66,L67 from SM070001R00 to SM070001N00.	For EMI's request
31.	02/23	P37	Change L56,L60,L71,L72 from SM070001U00 to SM070001R00.	For EMI's request
32.	02/23	P38,40	Add EC_MUTE_INT on UA1.48 and connected RB38 to UB1.122	For audio codec
33.	02/23	P9,40	Change UB1.123 from CLK_EC to CLK_EC_R and connected to RB7 and a reserve resistor RB5; and RB5 connected to CLK_EC; and RB7 connected to POK	For CLK_EC and POK
34.	02/27	P31	Change RT118, RT119, RT115, RT116 from @ to CRT@.	For DP to CRT vendor's recommend

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/19	Deciphered Date 2015/04/19	Title: HW-PIR-2

Size: D25 Custom	Document Number		Rev 1.0
Date: Tuesday, March 19, 2013	Sheet 54 of 53		